PRELIMINARY DATASHEET

CGY2136UH/C1

40-46 GHz 33dBm High Power Amplifier

DESCRIPTION

The CGY2136UH/C1 is a high performance GaAs Power Amplifier MMIC designed to operate in the millimeter Band.

The CGY2136UH/C1 has an output power of 2W at the 1dB compression point and has a small signal gain of 20dB. It can be used in Radar, telecommunication and instrumentation applications.

The CGY2136UH/C1 is a 3 stages dual line-up architecture with lange couplers for power splitting and combining delivering excellent input and output matching.

The die is manufactured using OMMIC's High Performance 0.13µm gate length PHEMT Power Technology D01PH. The MMIC uses gold bonding pads and backside metallization, the die is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

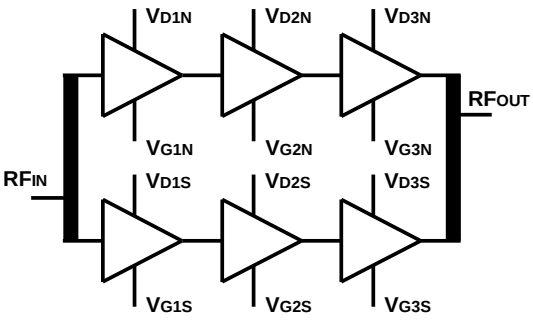
This technology has been evaluated for space applications and is on the European Preferred Parts List of the European Space Agency

APPLICATIONS

- Radar
- Telecommunications
- Instrumentation

FEATURES

- Operating frequency range : 40 to 46 GHz
- Output P_{sat} : 2.2 W (+ 33.5 dBm)
- Output P_{1dB} : 2.0 W (+ 33 dBm)
- Gain : 20dB
- 50 Ohms input and output matched
- Input Return Loss : > 10dB
- Output Return Loss : > 12dB
- Power Supply : 2.6A at 4.5V
- Delivered as 100 % on-wafer RF tested dies
- Samples and evaluation Boards Available
- Die size = 4.3 x 5.0 x 0.1 mm
- Device Availability (Q3 2011)
  - Tested, Inspected Known Good Die (KGD)
  - Module
  - Demonstration Boards
  - Space and MIL-STD MMIC's



CGY2136UH/C1 High Power Amplifier Block Diagram

RoHS Compliant

OMMIC

Revision : 03/12/2013

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MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1N}, V_{G2N}, V_{G3N}, V_{G1S}, V_{G2S}, V_{G3S}	Gate voltage		- 2,5	0	V
V_{D1N}, V_{D2N}, V_{D3N}, V_{D1S}, V_{D2S}, V_{D3S}	Drain voltage		0	+ 5.5	V
I_{D1N}, I_{D1S}	Drain current			300	mA
I_{D2N}, I_{D2S}				600	
I_{D3N}, I_{D3S}				800	
$I_{GNN, S}$ (all gates)	Gate Current		- 1	+ 1	mA
P_{IN}	RF Input power			+ 20	dBm
T_{amb}	Ambient temperature		- 40	+ 85	°C
T_j	Junction temperature			+ 175	°C
T_{stg}	Storage temperature		- 55	+ 85	°C

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j\ -\ amb)}$	Thermal resistance from junction to ambient (DC power at T_{amb} max)	TBD	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, $I_{D3N, D3S}$ = 640mA, $I_{D2N, D2S}$ = 440mA, $I_{D1N, D1S}$ = 200mA,

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RFin	Input frequency		40		46	GHz
Performances on Reference Board at f_i = 45 GHz						
$V_{D1N, 2N, 3N}$ $V_{D1S, 2S, 3S}$	Drain Supply voltage			+ 4,5		V
I_{DD}	Total supply current @ Psat			2600		mA
G	Gain			20		dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point		+32.5			dBm
Psat	Saturated power		+33.0			dBm
PAE	Power Added Efficiency			18		%
OIP3	Output third order intercept point			+ 41		dBm
IMD3	2 Carriers 3 dB below P1dB			TBD		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT}/RF_{IN}		-40		dB
S_{11}	Input reflection coefficient	50 Ohms	-10			dB
S_{22}	Output reflection coefficient	50 Ohms	-12			dB
P_{OFF}	Leakage when HPA off All gates = -2,5V	RFIN = + 17 dBm		TBD		dBm

(*) Measurement reference planes are the INPUT and OUTPUT plans of the CGY2136UH MMIC.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

S-PARAMETERS

Conditions : $V_{D3N,D3S}$ = $V_{D2N, D2S}$ = $V_{D1N, D1S}$ = 4.5V, ($I_{DQ3N, IDQ3S}$ = 640mA, $I_{DQ2N, IDQ2S}$ = 440mA, $I_{DQ1N, IDQ1S}$ = 200 mA), T_{amb} = + 25°C (On Wafer measurements)

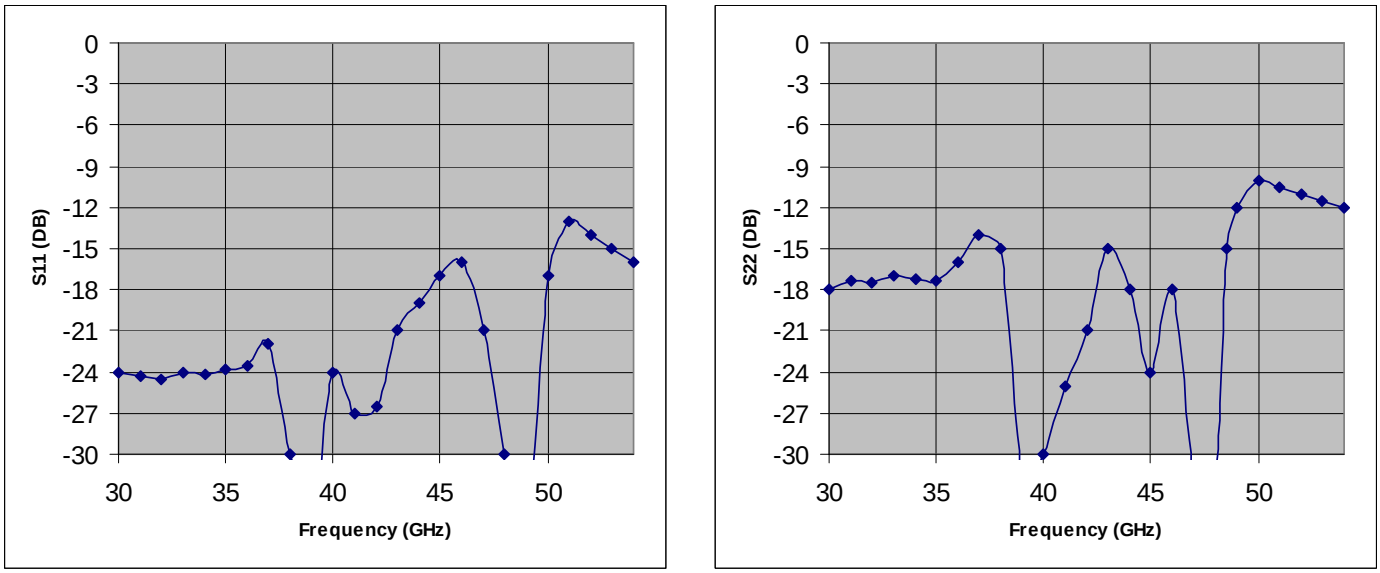

Figure 1 Input and output matching vs frequency

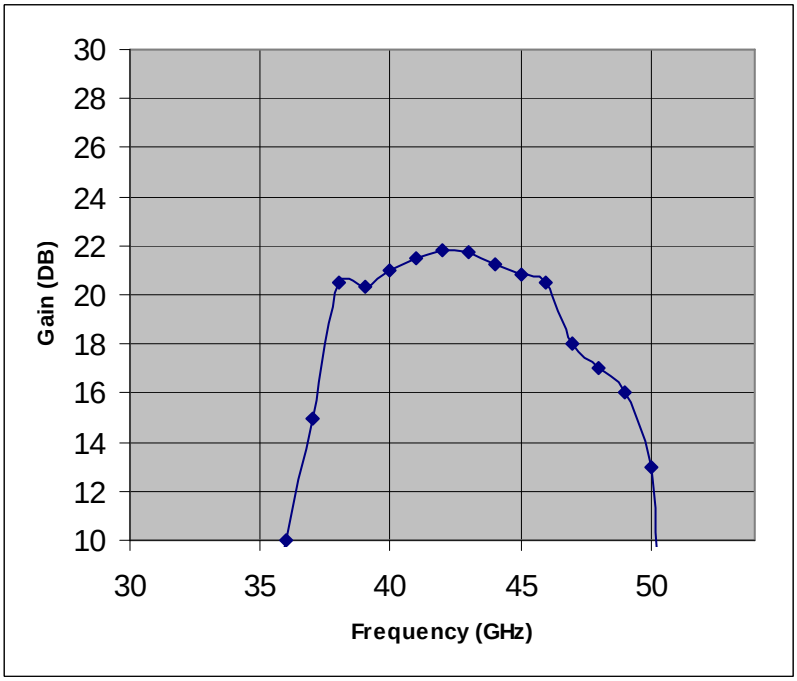

Figure 2 Gain vs frequency

GAIN CURVE

Conditions : $V_{D3N,D3S}$ = $V_{D2N, D2S}$ = $V_{D1N, D1S}$ = 4.5V, ($I_{DQ3N, DQ3S}$ = 640mA, $I_{DQ2N, DQ2S}$ = 440mA, $I_{DQ1N, DQ1S}$ = 200 mA), T_{amb} = + 25°C (On Wafer measurements)

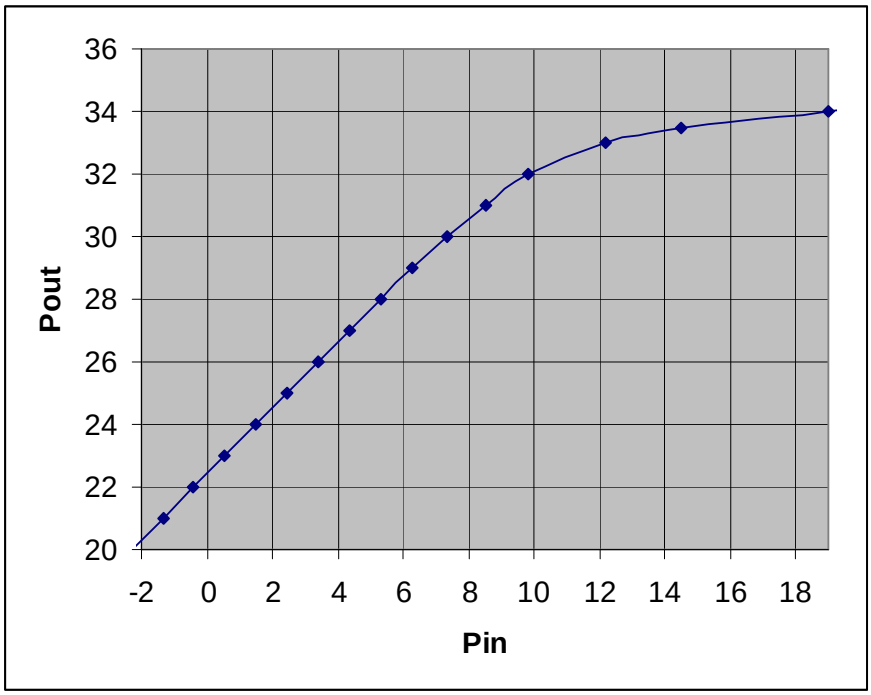

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Figure 3 Pout vs Pin @45GHz

1DB COMPRESSION POINT, SATURATED POWER AND PAE

Conditions : V_{D3N}, V_{D3S} = V_{D2N}, V_{D2S} = V_{D1N}, V_{D1S} = 4.5V, I_{DQ3N}, I_{DQ3S} = 640mA, I_{DQ2N}, I_{DQ2S} = 440mA, I_{DQ1N}, I_{DQ1S} = 200 mA, T_{amb} = + 25°C (On Wafer measurements)

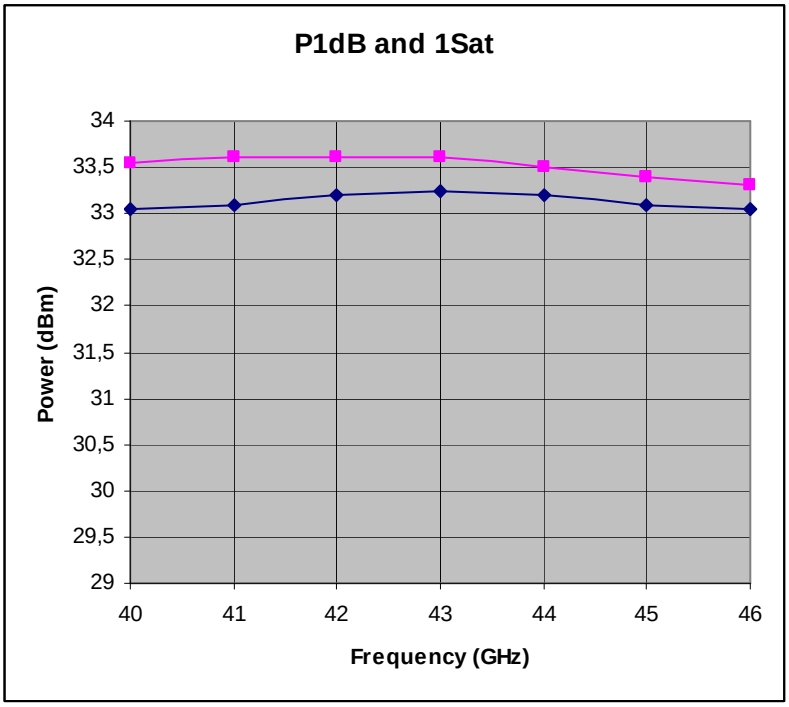


Figure 4 P1dB and Psat vs frequency

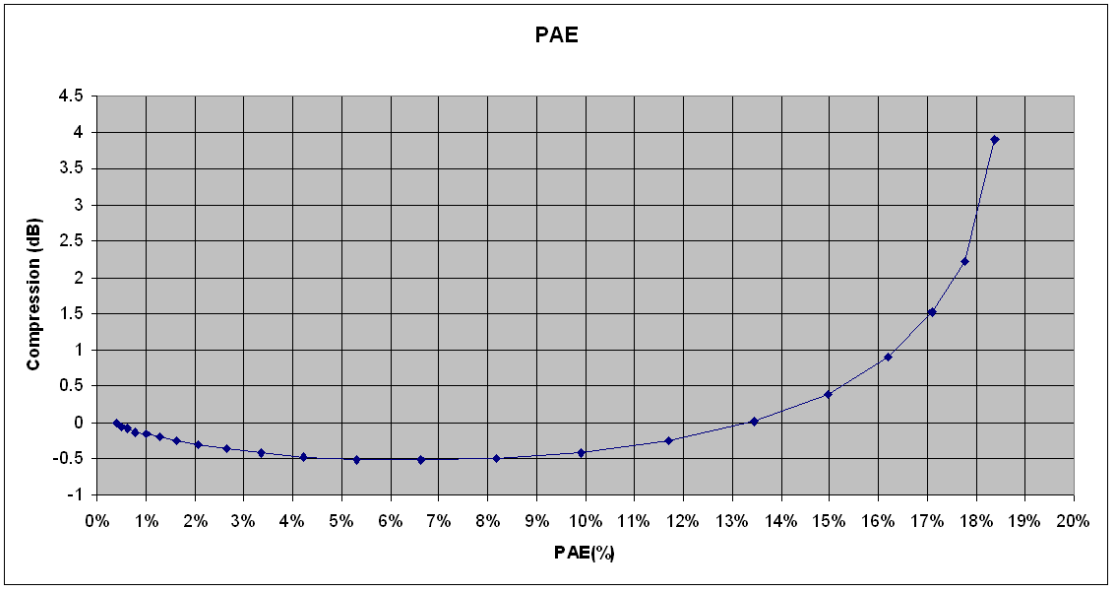


Figure 5 PAE vs compression

APPLICATION SCHEMATIC

To prevent unstability of the customer design it is hightly recommended to place a 47pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionnaly, a 10nF capacitor can be added on a drain connection. In the gate circuitry, a 500 Ω resistor have been added in serie with each gate introducing some low pass filtering in case of fast power switching.

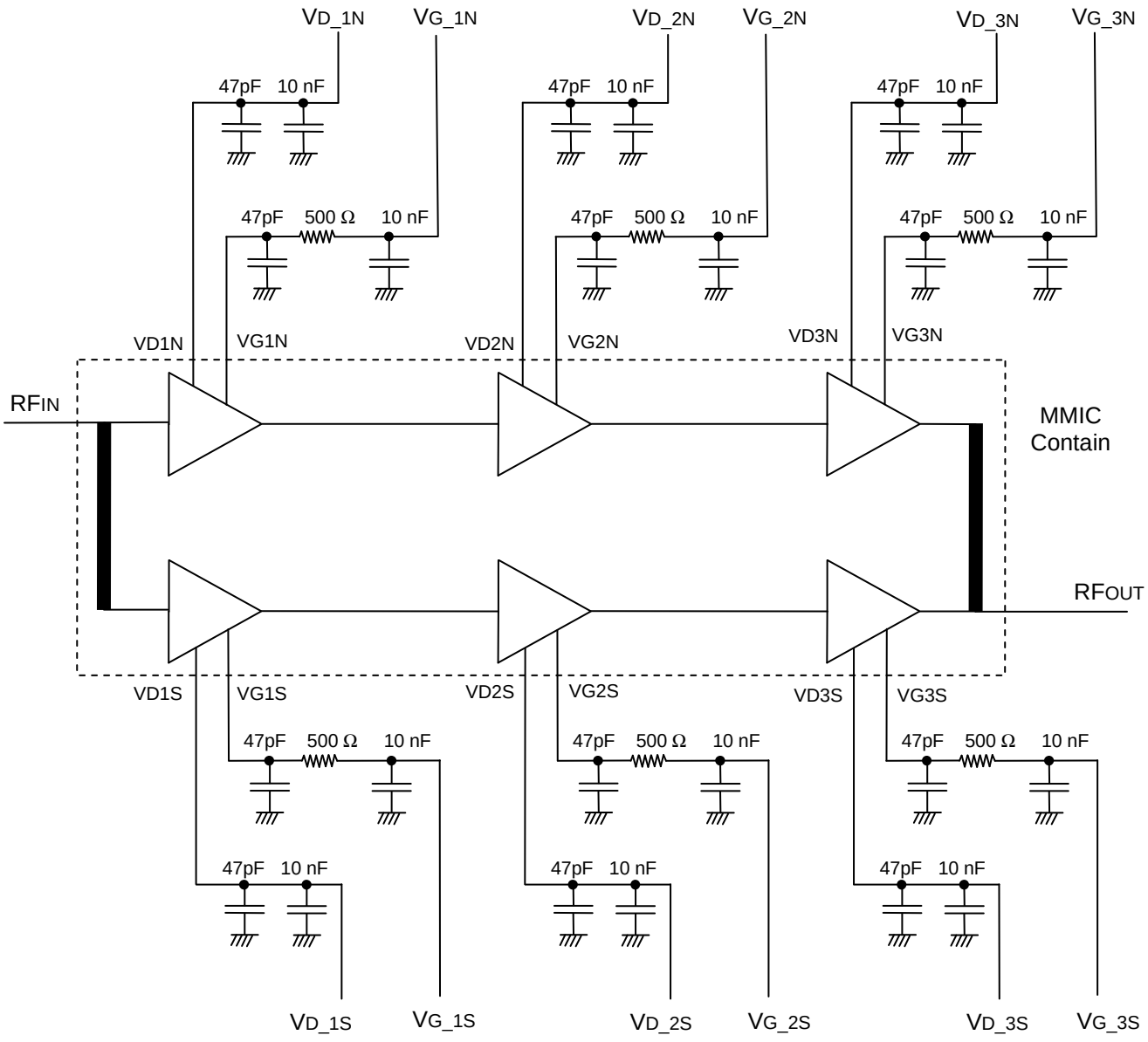


Figure 6 : Application schematics

Component NAME	Value	Type	Comment
All 47pF capacitors	47pF	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die with bonding as short as possible

All 500 Ω resistors	500 Ω	Chip Resistor	Chip resistor US MICROWAVES RG1421-500-1% soldered close to the 47pF chip capacitor with bonding as short as possible
All 10nF capacitors	10nF	Chip Capacitor	MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520

Due to the highly symmetrical design of the component and the requirements of the power combiner, it is recommended to keep I_{DQ1N} equal to I_{DQ1S}, I_{DQ2N} equal to I_{DQ2S} and I_{DQ3N} equal to I_{DQ3S}, for the same reason, it is recommended to keep V_{D1N} equal the V_{D1S}, V_{D2N} equal the V_{D2S} and V_{D3N} equal the V_{D3S}.

In order to save DC power consumption and improve PAE each of the 6 gates can be individually driven at a different bias voltage. In this case, when using the targeted RF signal (modulated carrier), the distortion is monitored while adjusting V_{G1N},V_{G2N}, V_{G3N}, V_{G1S}, V_{G2S} and V_{G3S}. The global strategy is to introduce all the distortion allowed by the targeted standard in the last stage of the amplifier by adjusting V_{G3N}, V_{G3S} while V_{G1N}, V_{G1S}, V_{G2N}, V_{G2S} are positioned in such a way that the 2 first stages of each line-up are kept at a neglectable contribution to the global distortion.

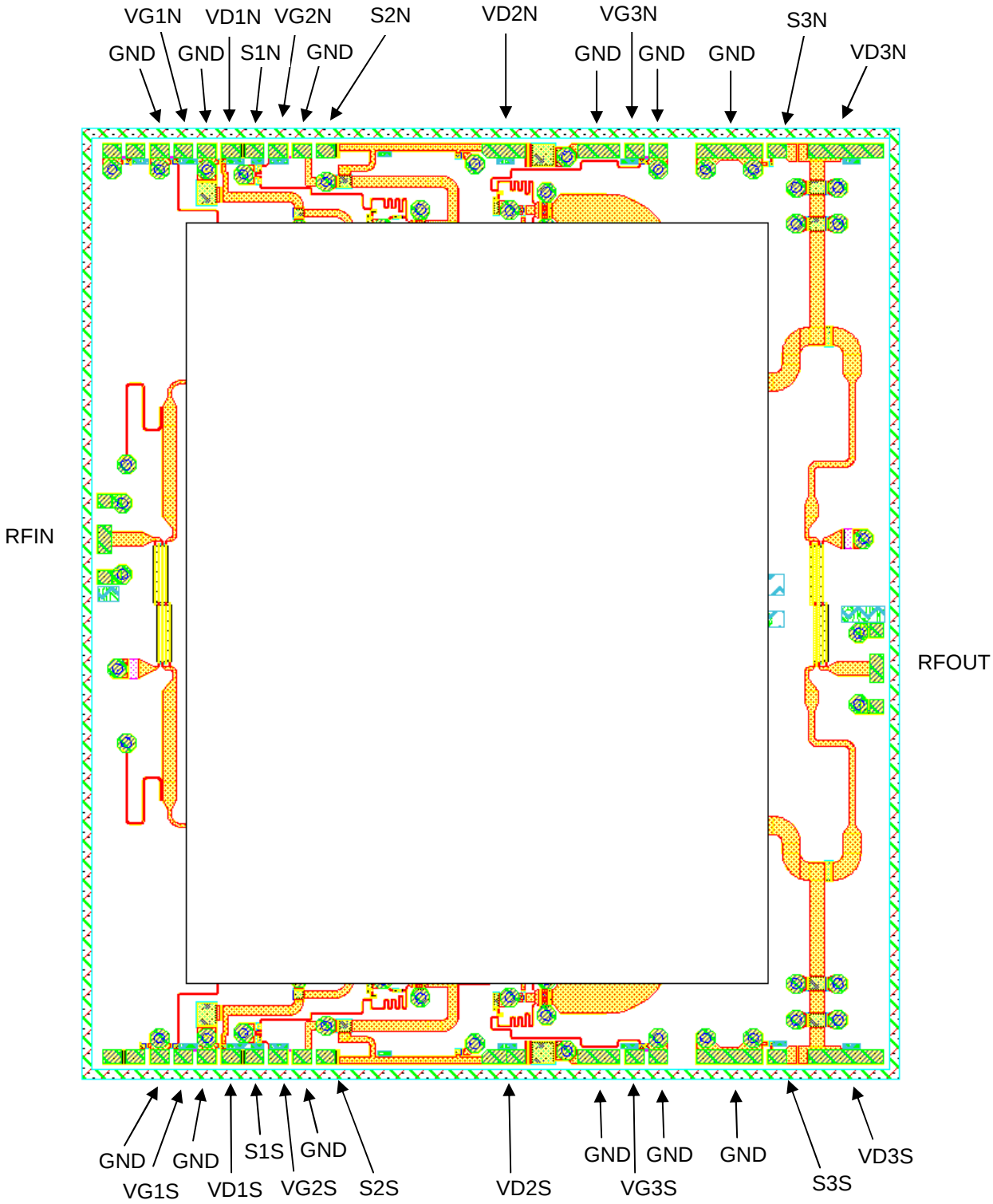
An additional amount of DC power supply can be saved in fine tuning the drain voltages V_{D1N},V_{D2N}, V_{D3N}, V_{D1S}, V_{D2S} and V_{D3S} while following the same procedure and the same strategy as described above.

In order to validate each stage of the amplifier, with respect to the DC, it is recommended to set V_{GXS} or $V_{GXN\ (X=1,2,3)}$ to -2.5V, then to set first the corresponding drain voltage V_{DXS} or $V_{DXN\ (X=1,2,3)}$ to +1V and check that the corresponding I_{DXS} or $I_{DXN\ (X=1,2,3)}$ drain current stay at a very low level, after that verification, V_{DXS} or $V_{DXN\ (X=1,2,3)}$ can be set to 4.5V. When V_{GXS} or $V_{GXN\ (X=1,2,3)}$ is changed from -2.5 to -0.3V, the corresponding drain current I_{DXS} or $I_{DXN\ (X=1,2,3)}$ increases slowly in a controlled manner to reach the typical targeted value.

Each gate can be randomely and independently positionned, no particular order is required.

DIE LAYOUT AND PIN CONFIGURATION

In order to enable to access voltage drain, an additionnal sense pad have been implemented on each drain voltage. The customer is free to use it or not.



PINOUT

The amplifier has a North and South face, North is top and South is Bottom when RF input is on the left and RF output on the right.

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD1N	VD1N	First stage Drain (amplifier North)
VD2N	VD2N	Second stage Drain (amplifier North)
VD3N	VD3N	Third stage Drain (amplifier North)
S1N	Sense VD1N	First stage Drain Sense (amplifier North)
S2N	Sense VD2N	Second stage Drain Sense (amplifier North)
S3N	Sense VD3N	Third stage Drain Sense (amplifier North)
VG1N	VG1N	First stage Gate (amplifier North)
VG2N	VG2N	Second stage Gate (amplifier North)
VG3N	VG3N	Third stage Gate (amplifier North)
VD1S	VD1S	First stage Drain (amplifier South)
VD2S	VD2S	Second stage Drain (amplifier South)
VD3S	VD3S	Third stage Drain (amplifier South)
S1S	Sense VD1S	First stage Drain Sense (amplifier South)
S2S	Sense VD2S	Second stage Drain Sense (amplifier South)
S3S	Sense VD3S	Third stage Drain Sense (amplifier South)
VG1S	VG1S	First stage Gate (amplifier South)
VG2S	VG2S	Second stage Gate (amplifier South)
VG3S	VG3S	Third stage Gate (amplifier South)
GND	BACKSIDE	Ground

Note :

In order to ensure good RF performances and stability It is key to connected to the ground the pad available on the backside of the die.

BONDINGS PAD COORDINATES

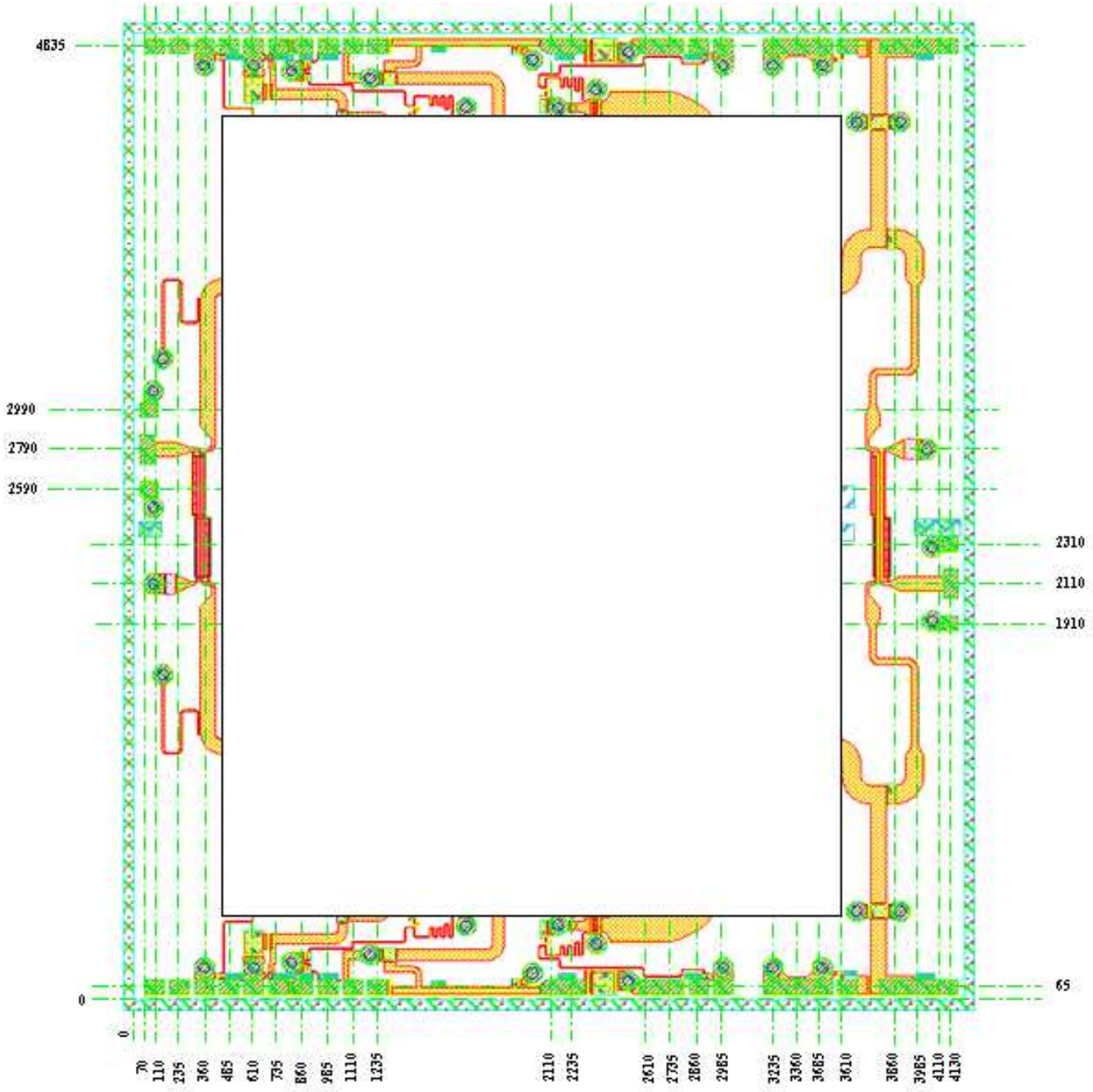


Figure 7 Bondings pad coordinates

MMIC Steps on the wafer are 4.3 and 5.0 mm along X and Y coordinated respectively, dicing typically reduce the die size by 30um.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on-wafer tested	32	-	4.3 x 5.0 x 0.1

SOLDERING

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330℃.

Temperature in excess of 300℃ should not be applie d to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400℃

ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2136	UH	C1	-	On-Wafer measured Die

RoHS Compliant

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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