PRELIMINARY DATASHEET

CGY2139AUH/C1

8-12 GHz 41dBm Power Amplifier

DESCRIPTION

The CGY2139AUH/C1 is a high performance dual line-up 3 stages GaAs Power Amplifier MMIC designed to operate in the X band.

The CGY2139AUH/C1 has an output power of 10 W at the 1dB compression point and has a small signal gain of 21 dB. It can be used in X-band Radars, Telecommunication and Instrumentation applications.

The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

The MMIC power dissipation is limited by the die thermal resistance, it has been designed to work in pulse mode, The CGY2139AUH/C1 can be operated at a duty cycle as high as 50%. Drain switch mode is the preferred control mode.

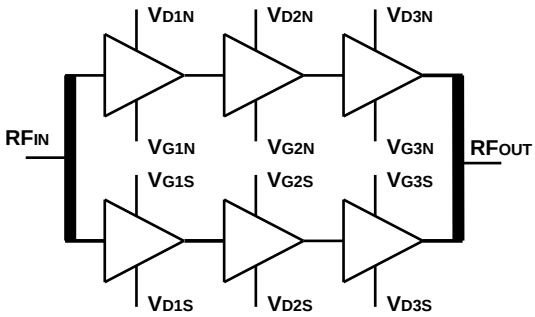
Cascading CGY2139PUH/C1 or CGY2139MUH/C1 with CGY2139AUH/C1 can form a 40dB gain 10W X-band pulse mode amplifier chain.

APPLICATIONS

- Radar
- Telecommunications
- Instrumentation

FEATURES

- Operating Range : 8 GHz to 12 GHz
- Output P_{sat} : 40.5 dBm
- Output P_{1dB} : 40 dBm
- Gain : 21 dB
- 50 Ohms input and output matched
- Input Return Loss : > 10 dB
- Output Return Loss : > 10 dB
- Power Supply : 4.9 A at VDD = 8 V
- Die size = 4.5 x 4.1 x 0.1 mm
- Device Availability (Q2 2012) :
  - Tested, Inspected Known Good Die (KGD)
  - Connectorized evaluation solution



CGY2139AUH/C1 Block Diagram

RoHS Compliant

Revision : 04/12/2013

OMMIC

2, Rue du Moulin – BP11 – 94 453

Limeil-Brévannes Cedex – France.

Website : www.ommic.com

Email : information@ommic.com

MAXIMUM VALUES

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1N}, V_{G2N}, V_{G3N}, V_{G1S}, V_{G2S}, V_{G3S}	Gate voltage		- 2,5	0	V
V_{D1N}, V_{D2N}, V_{D3N}, V_{D1S}, V_{D2S}, V_{D3S}	Drain voltage		0	+ 9	V
I_{D1N}, I_{D1S}	Drain current			200	mA
I_{D2N}, I_{D2S}				600	
I_{D3N}, I_{D3S}				1800	
$I_{GNN, S}$ (all gates)	Gate Current		- 10	+ 10	mA
P_{IN}	RF Input power			+ 25	dBm
T_{amb}	Ambient temperature		- 40	+ 85	°C
T_j	Junction temperature			+ 175	°C
T_{stg}	Storage temperature		- 55	+ 85	°C

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j\ -\ amb)}$	Thermal resistance from junction to ambient (DC power at T_{amb} max)	TBD	°C/W

ELECTRICAL CHARACTERISTICS

Conditions : T_{amb} = + 25 °C, $I_{DQ3N, DQ3S}$ = 1400mA, $I_{DQ2N, DQ2S}$ = 400mA, $I_{DQ1N, DQ1S}$ = 125mA, 10% duty cycle

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RFin	Input frequency		8		12	GHz
Performances on Reference Board at f_i = 10 GHz						
$V_{D1N, 2N, 3N}$ $V_{D1S, 2S, 3S}$	Drain Supply voltage		8.0		9.0	V
I_{DD}	Total supply current @ Psat			4.3	5.0	A
G	Gain		21			dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point			40		dBm
Psat	Saturated power			40.5		dBm
PAE	Power Added Efficiency			36		%
OIP3	Output third order intercept point			50		dBm
IMD3	2 Carriers 3 dB below P1dB			TBD		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT}/RF_{IN}		TBD		dB
S_{11}	Input reflection coefficient	50 Ohms		-14		dB
S_{22}	Output reflection coefficient	50 Ohms		-15		dB
P_{OFF}	Leakage when HPA off All gates = -2,5V	RFIN = + 20 dBm		TBD		dBm

(*) Measurement reference planes are the INPUT and OUTPUT plans of the CGY2139AUH/C1 MMIC.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

CGY2139AUH/C1 can only be measured on-wafer using a pulse measurement test-bench, this method assure a full polarization conditions and cold channel temperature, this method also remove the risk of reliability damages due to high temperature overstress inherent to on wafer measurements at full polarization and reflects the performances of the devices in good cooling conditions.

S-PARAMETERS

Conditions : $V_{D3N,D3S}$ = $V_{D2N, D2S}$ = $V_{D1N, D1S}$ = 8.0V, ($I_{DQ3N, IDQ3S}$ = 1400mA, $I_{DQ2N, IDQ2S}$ = 400mA, $I_{DQ1N, IDQ1S}$ = 125 mA), T_{amb} = + 25°C (Simulation)

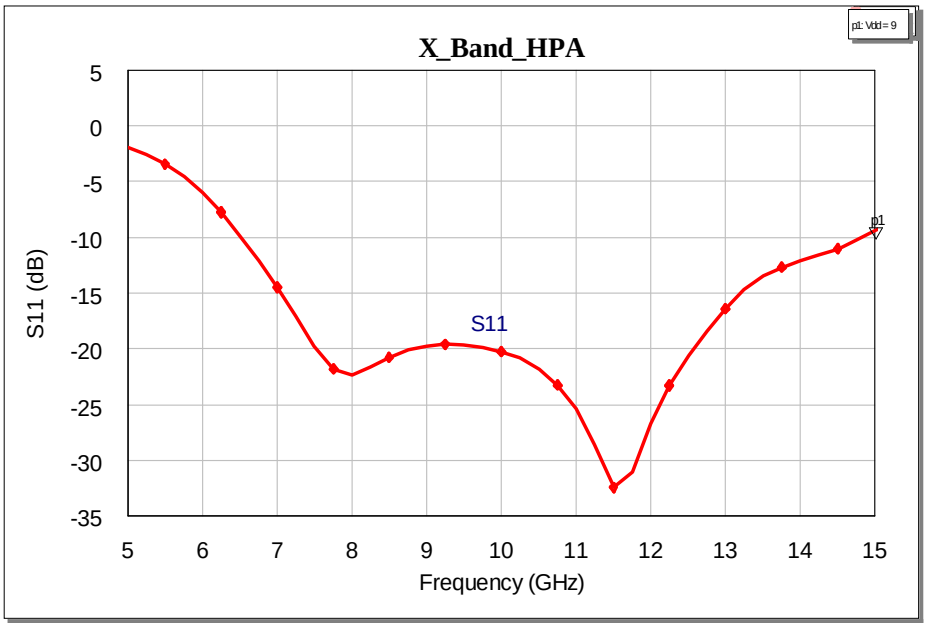


Figure 1 : S11 - Simulated

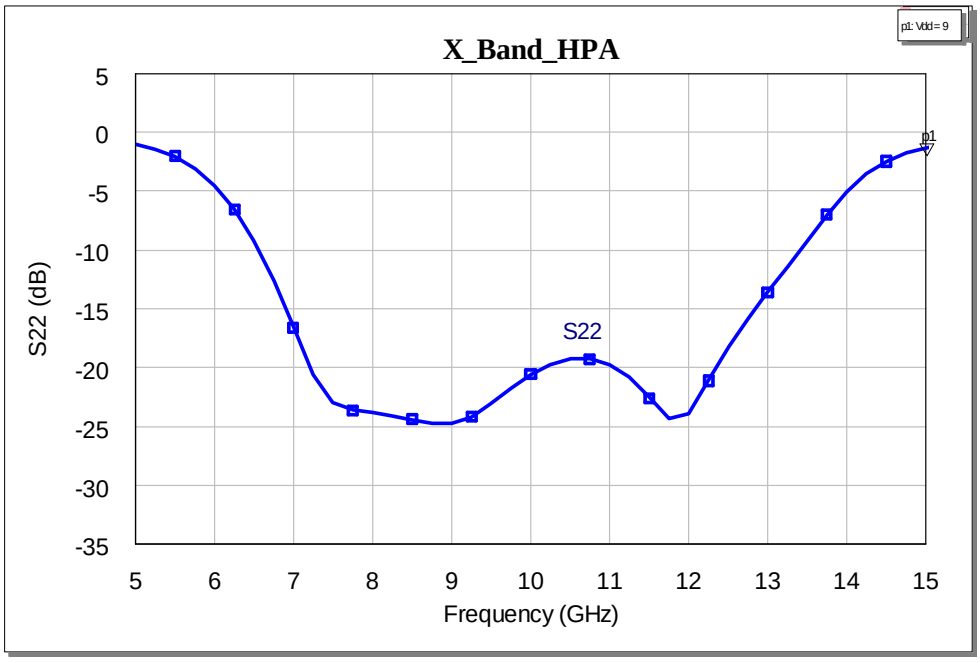


Figure 2 : S22 - Simulated

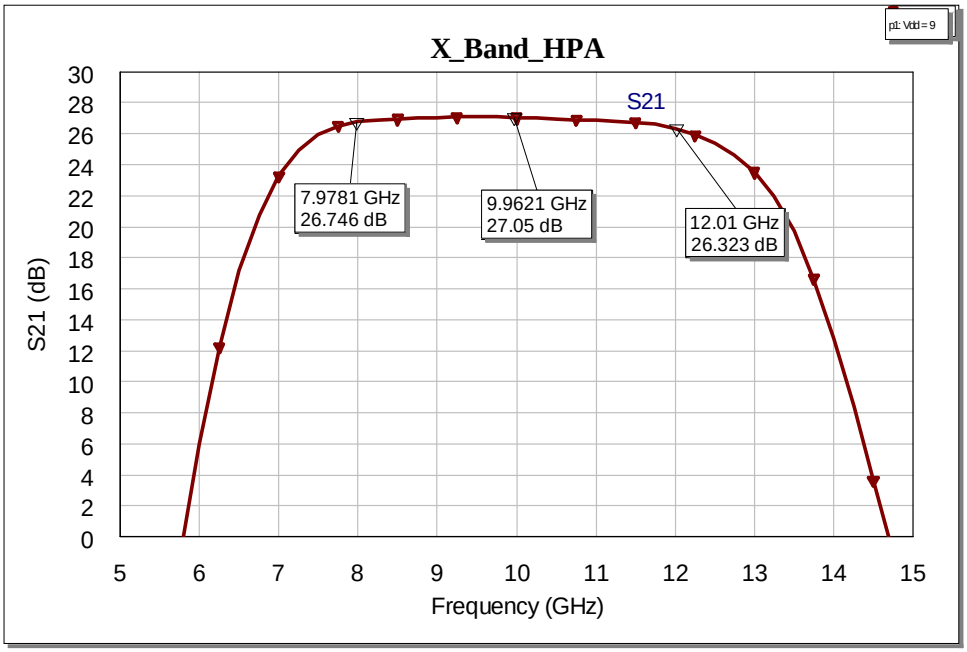


Figure 3 : S21 - Simulated

WIDE BAND S-PARAMETERS

Conditions : $V_{D3N,D3S}$ = $V_{D2N, D2S}$ = $V_{D1N, D1S}$ = 8.0V, ($I_{DQ3N, DQ3S}$ = 1400mA, $I_{DQ2N, DQ2S}$ = 400mA, $I_{DQ1N, DQ1S}$ = 125 mA), T_{amb} = + 25°C (Simulation)

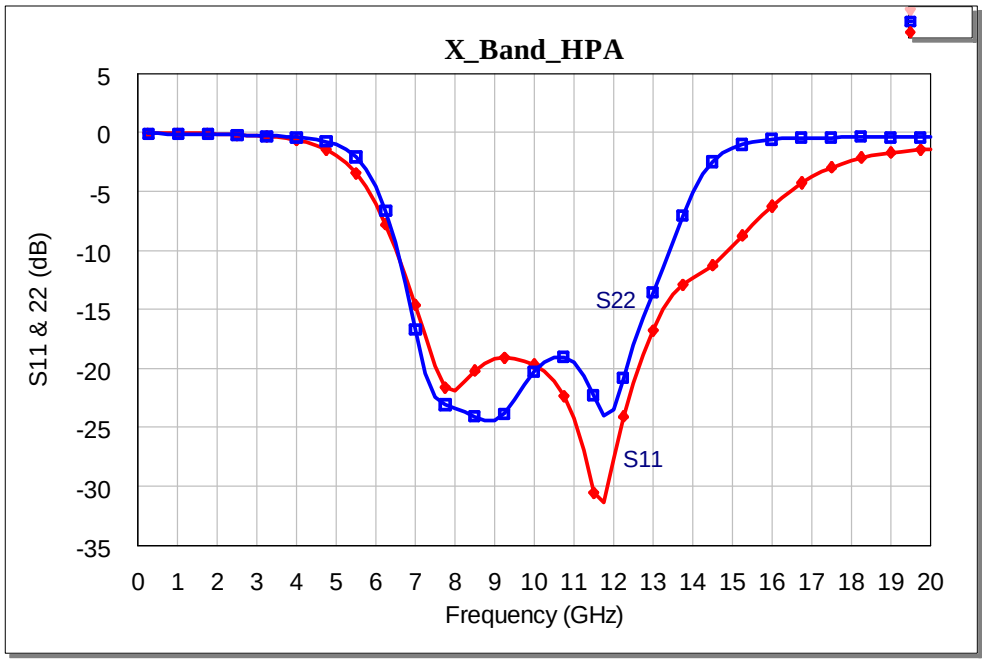


Figure 4 : S11 & S22 wide band S parameters - Simulated

CGY2139AUH/C1 have been designed to present a 50 Ohms plan at the die port. 2 to 3 standard wire bondings (25um in diameter 300um in length) can be used to connect the die to the environment (microstrip or coplanar). The wire bonding terminal (alumina or PCB substrate) should be build to compensate the inductance introduced by the wire bounding over the frequency band.

1DB COMPRESSION POINT, SATURATED POWER, PAE AND GAIN

Conditions : On Carrier measurements with 50 Ohms probes
V_{D3N}, V_{D3S} = V_{D2N}, V_{D2S} = V_{D1N}, V_{D1S} = 8.0V, V_{G3N}, V_{G3S} = V_{G2N}, V_{G2S} = V_{G1N}, V_{G1S} = -0.7V, (I_{DQ3N}, I_{DQ3S} = 1400mA, I_{DQ2N}, I_{DQ2S} = 400mA, I_{DQ1N}, I_{DQ1S} = 125 mA), duty cycle 10%, T_{amb} = + 25°C

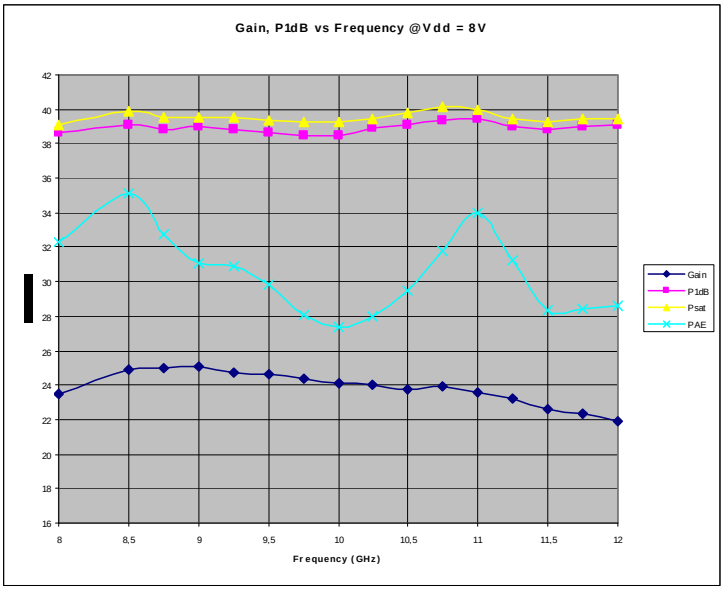


Figure 5 : CGY2139AUH/C1 Psat, Pout, Pae and Gain vs frequency

Conditions : On carrier wafer measurements with 50 Ohms probes
V_{D3N}, V_{D3S} = V_{D2N}, V_{D2S} = V_{D1N}, V_{D1S} = 8.5V, V_{G3N}, V_{G3S} = V_{G2N}, V_{G2S} = V_{G1N}, V_{G1S} = -0.7V, (I_{DQ3N}, I_{DQ3S} = 1400mA, I_{DQ2N}, I_{DQ2S} = 400mA, I_{DQ1N}, I_{DQ1S} = 125 mA), duty cycle 10%, T_{amb} = + 25°C

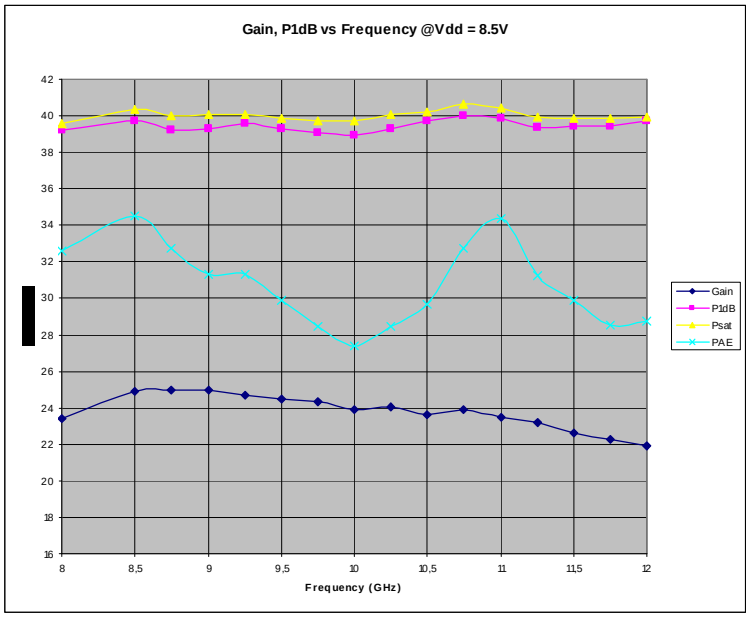


Figure 6 : Psat, Pout, Pae and Gain vs frequency

Conditions : On carrier wafer measurements with 50 Ohms probes
V_{D3N}, V_{D3S} = V_{D2N}, V_{D2S} = V_{D1N}, V_{D1S} = 9.0V, V_{G3N}, V_{G3S} = V_{G2N}, V_{G2S} = V_{G1N}, V_{G1S} = -0.7V, (I_{DQ3N}, I_{DQ3S} = 1400mA, I_{DQ2N}, I_{DQ2S} = 400mA, I_{DQ1N}, I_{DQ1S} = 125 mA), duty cycle 10%, T_{amb} = + 25°C

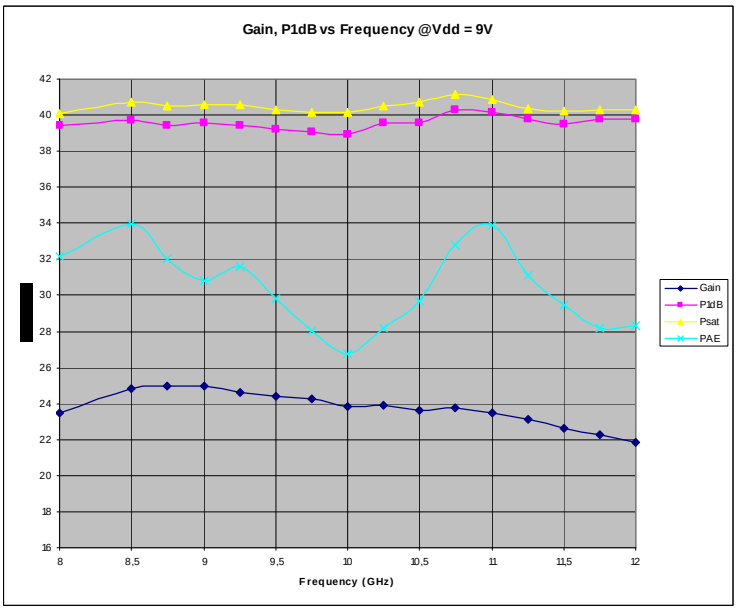


Figure 7 : CGY2139AUH/C1 Psat, Pout, Pae and Gain vs frequency

APPLICATION SCHEMATIC

Decoupling scheme depend on customer implementation, in order to prevent unstability it is hightly recommended to place a 47pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionnaly, a 10nF chip capacitor can be added on the drain 3 connection.

The decoupling network depends on supply, on grounding environement, on form factor, on all parasitics added by the customer environement. According to this, the appropriate network sometimes need to be fine-tuned in accordance with rules applyable in the high frequency domain.

It may also be required to add very low frequency, high capacitor value, on each drain a 10 Ohms + 10 nF RC serie network made of 0402 format capacitors as it has been done in the reference test-jig.

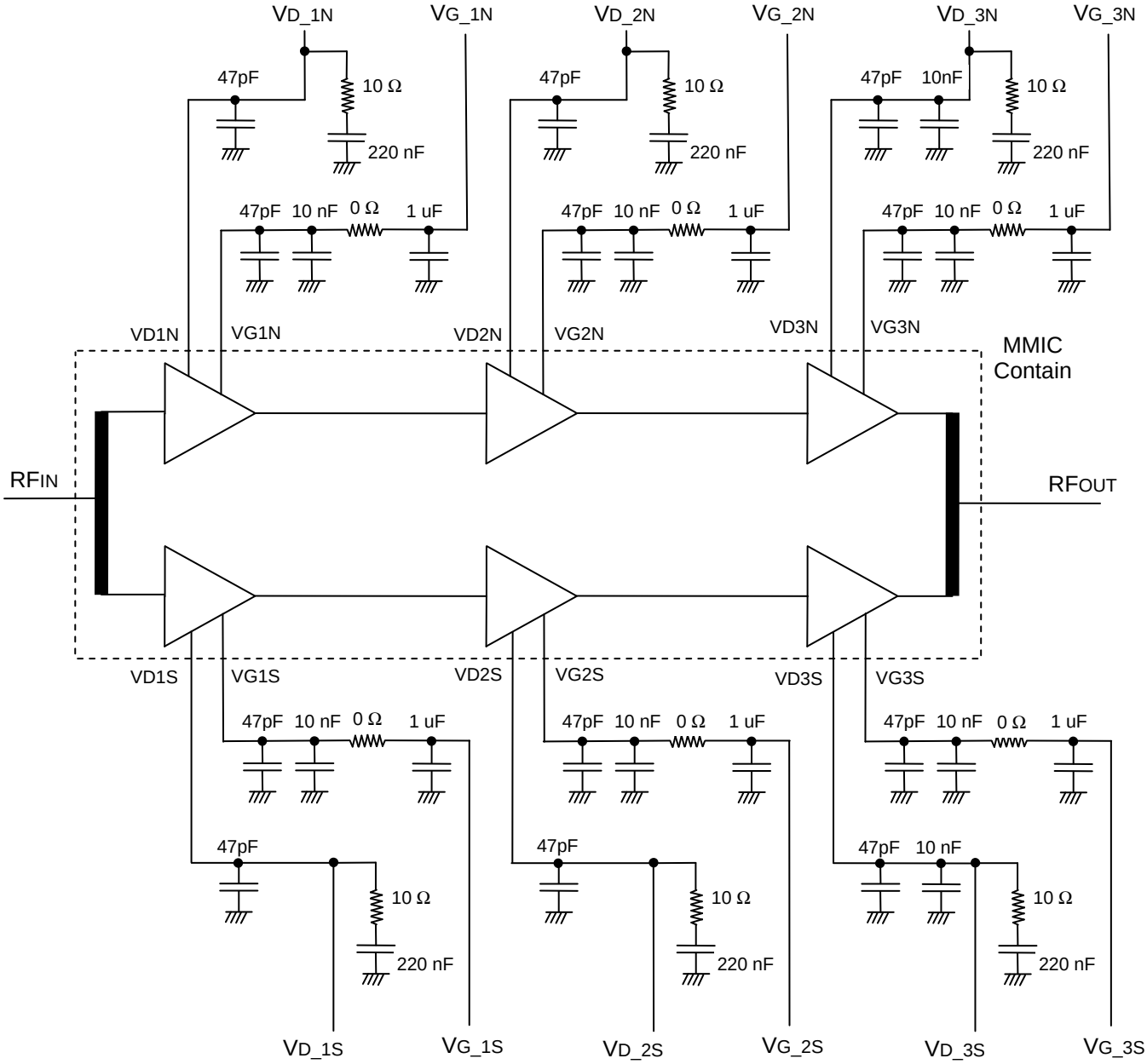


Figure 8 : CGY2139AUH/C1 Application schematics

Component NAME	Value	Type	Comment
All 47pF capacitors	47pF	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die with bonding as short as possible
All 10nF capacitors	10nF	Chip Capacitor	MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520

Due to the highly symmetrical design of the component and the requirements of the power combiner, it is recommended to keep the supply design as symmetrical as possible, this means I_{DQ1N} equal to I_{DQ1S}, I_{DQ2N} equal to I_{DQ2S} and I_{DQ3N} equal to I_{DQ3S}, for the same reason, it is recommended to keep V_{D1N} equal the V_{D1S}, V_{D2N} equal the V_{D2S} and V_{D3N} equal the V_{D3S}. It is important to keep V_{G1N} equal the V_{G1S}, V_{G2N} equal the V_{G2S} and V_{G3N} equal the V_{G3S}.

CGY2139AUH/C1 can be supplied with only a single pulsed Vd voltage and only a single Vg voltage. Nevertheless, it is very important to keep efficient decoupling networks on drain and gates. Improper decoupling networks can lead to oscillations through supply guided feedback loop.

CGY2139AUH/C1 have been designed to present a 50 Ohms plan at the die port. 2 to 3 standard wire bondings (25um in diameter 300um in length) can be used to connect the die to the environment (microstrip or coplanar). The wire bonding terminal (alumina or PCB substrate) should be build to compensate the inductance introduced by the wire bounding over the frequency band.

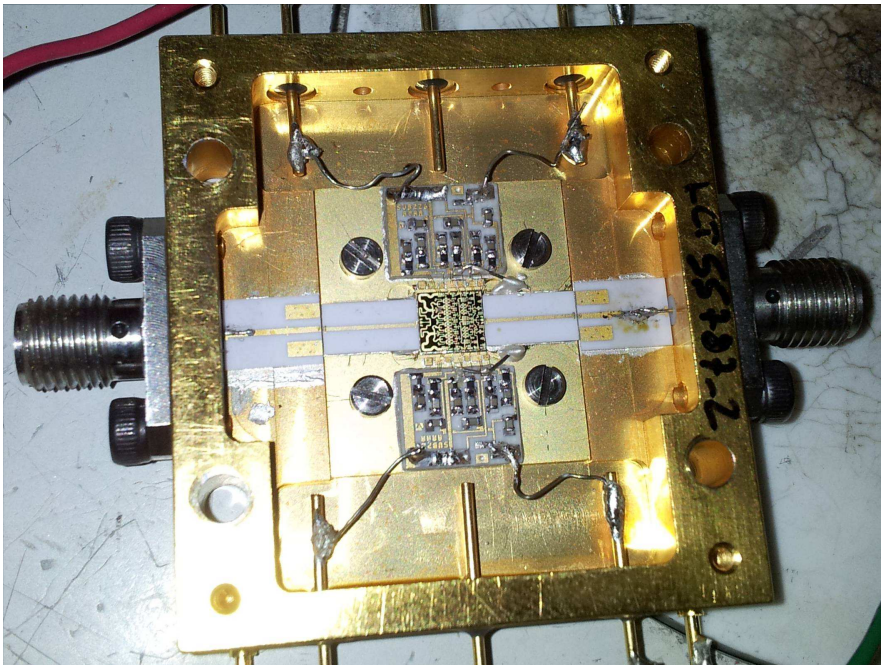
As the use of different Vg on each stage can be used to optimize a particular parameter corresponding to customer demand, all Vg are left available for customer.

CW OPERATIONS

CGY2139AUH/C1 doesn't support CW operation at full bias, reducing Idd with Vg can be done, Idd reduced by 50% can be accepted in CW operation. VDD = 5V with IDD = 2.5A with 5W output power can be reach with appropriately designed cooling environement.

TEST JIG

A Connecteurized test-jig have been developped, a picture is showed below.



The test-jig add losses, here below are narrow and large band plots of input return loss and attenuation

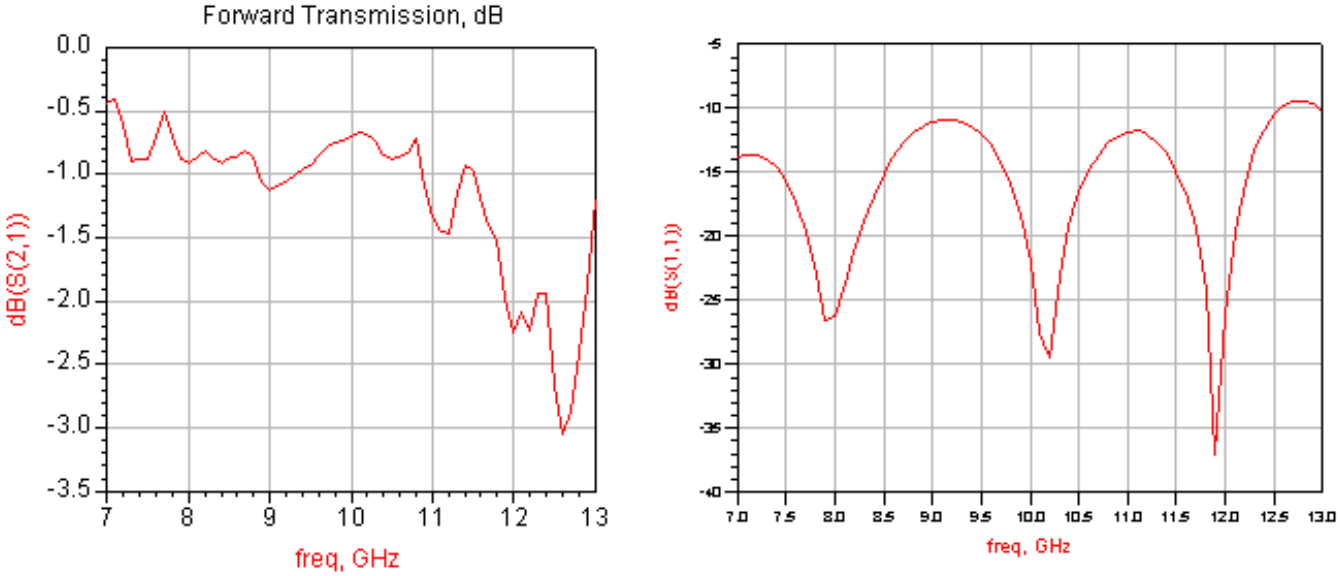


Figure 9 : Insertion loss and input return loss of thest-jig

The following results have been captured in the test-jig environment within connector plan, the through evaluation provide a basis to de-embedded the housing an come back in the die plan which is the OMMIC reference plan.

The figure below is showing the gain of the HPA (in SMA housing) versus the input power for different values of the operating frequency.

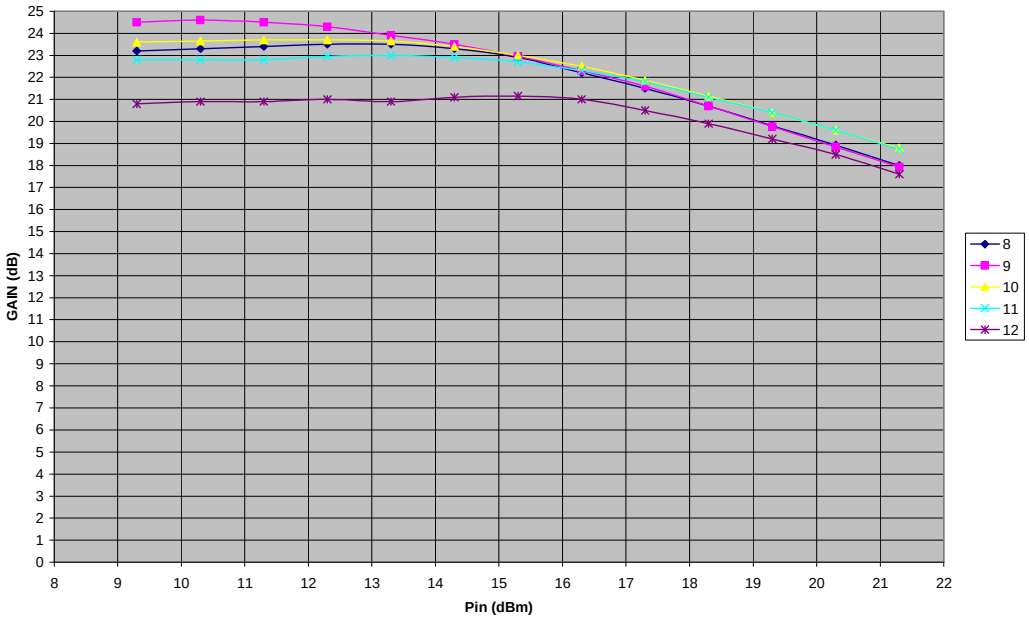


Figure 10 : Gain Vs Input power for VD=8.5V, VG=-0.7V and for different values of the frequency

The figure below is showing the output power of the HPA (in SMA housing) versus the input power for different values of the operating frequency.

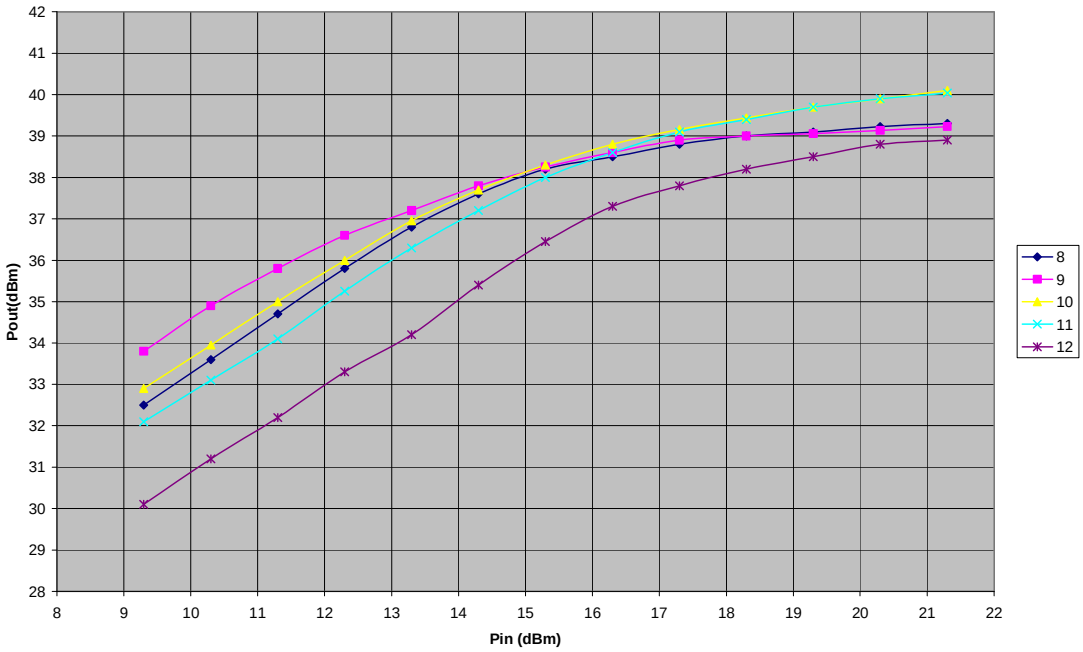


Figure 11 : Output power Vs Input power for VD=8.5V, VG=-0.7V and for different values of the frequency

The figure below is showing the current consumption of the HPA (in SMA housing) versus the input power for different values of the operating frequency. We can observe that the current is variable between 3A and 4.3A for operating frequency from 8GHz to 12GHz.

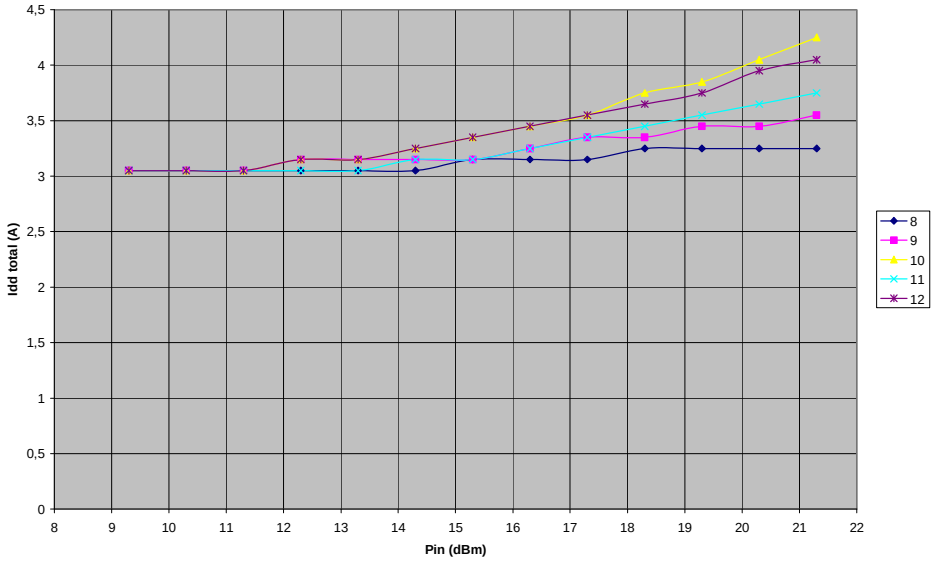


Figure 12 : Current consumption Vs Input power for VD=8.5V, VG=-0.7V and for different values of the frequency.

DIE LAYOUT AND PIN CONFIGURATION

The Die is symetrical on the RF axis. The die positionned top view with RF input on the left and RF output on the right show DC accesses on the top labelled north (N) and DC accesses on the bottom labelled south (S). V_{D1N}, V_{D2N}, V_{D3N}, V_{G1N}, V_{G2N}, V_{G3N} are DC signals applied on the north side, V_{D1S}, V_{D2S}, V_{D3S}, V_{G1S}, V_{G2S}, V_{G3S} are DC signals applied on the south side. Many ground accesses are complementing the pad layout. The backside is the ground reference plan.

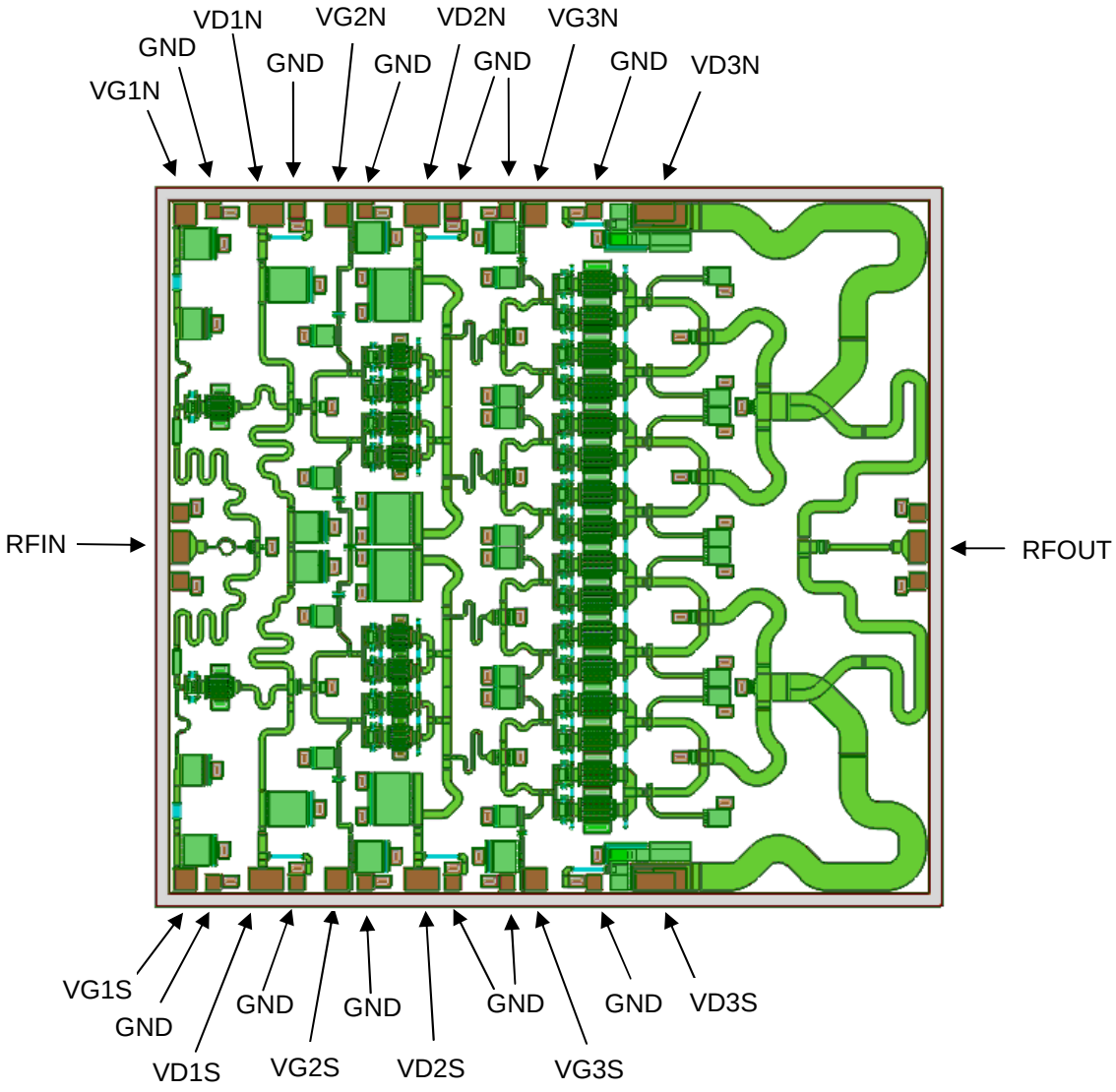


Figure 13 : CGY2139AUH/C1 Pad layout

PINOUT

The amplifier has a North face and a south face, north is top and south is bottom when RF input is on the left an RF output on the right.

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD1N	VD1N	First stage Drain (amplifier North)
VD2N	VD2N	Second stage Drain (amplifier North)
VD3N	VD3N	Third stage Drain (amplifier North)
VG1N	VG1N	First stage Gate (amplifier North)
VG2N	VG2N	Second stage Gate (amplifier North)
VG3N	VG3N	Third stage Gate (amplifier North)
VD1S	VD1S	First stage Drain (amplifier South)
VD2S	VD2S	Second stage Drain (amplifier South)
VD3S	VD3S	Third stage Drain (amplifier South)
VG1S	VG1S	First stage Gate (amplifier South)
VG2S	VG2S	Second stage Gate (amplifier South)
VG3S	VG3S	Third stage Gate (amplifier South)
GND	BACKSIDE	Ground

Note :

In order to ensure good RF performances and stability It is key to connect to the ground the pad available on the backside of the die.

BONDINGS PAD COORDINATES

Symbol	X coordinate (um)	Y coordinate (um)	Pad size (um x um)
GND	90	1850	Ground pad associated with RF input
RFIN	90	2050	100 x 190
GND	90	2250	Ground pad associated with RF input
VG1N	115	3995	130 x 130
GND	280	4015	90 x 90
VD1N	595	3995	200 x 130
GND	771	4015	90 x 90
VG2N	1005	3995	130 x 130
GND	1170	4015	90 x 90

VD2N	1506	3995	200 x 130
GND	1684	4015	90 x 90
GND	2005	4015	90 x 90
VG3N	2170	3995	130 x 130
GND	2522	4015	90 x 90
VD3N	2914	3995	300 x 100
GND	4410	1850	Ground pad associated with RF output
RFOUT	4410	2050	100 x 190
GND	4410	2250	Ground pad associated with RF output
GND	BACKSIDE		Ground

Tableau 1 CGY2139AUH/C1 Pad size and coordinates

BONDINGS PAD DRAWING

MMIC Steps on the wafer are 4.5 and 4.1 mm along X and Y coordinated respectively, dicing typically reduce the die by 30um.

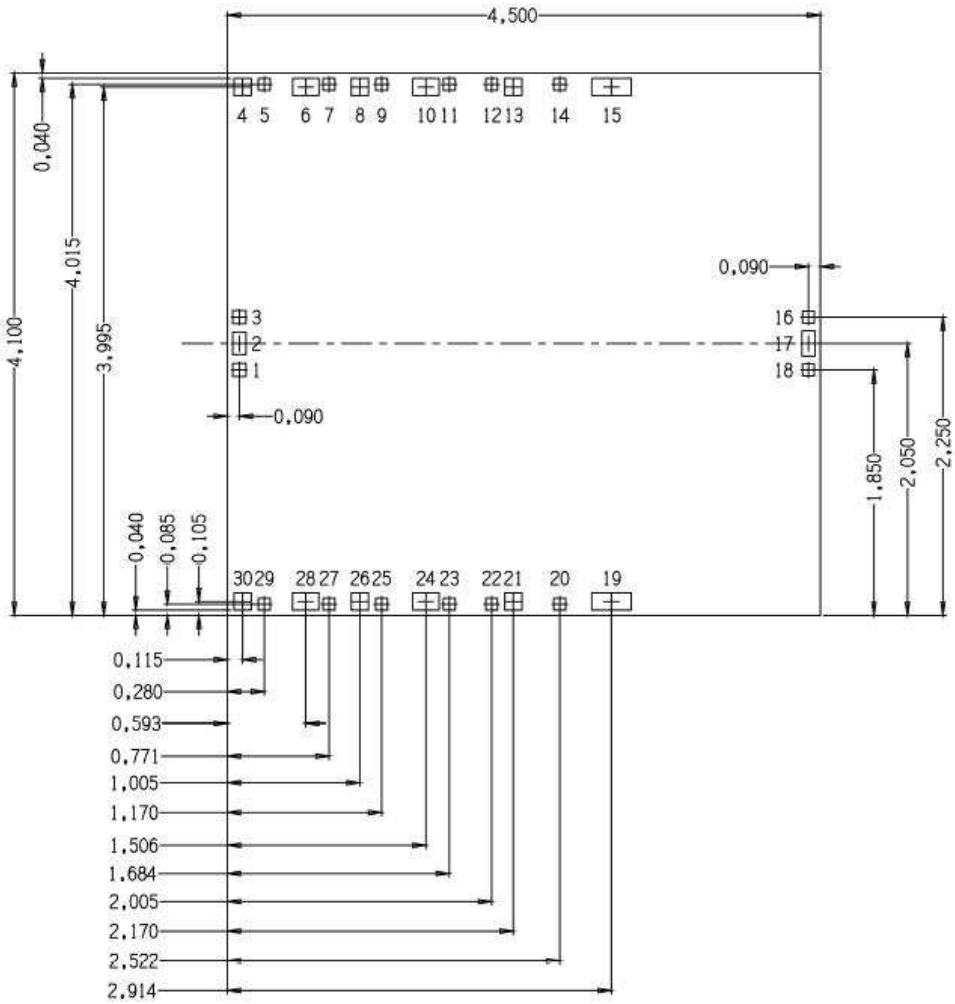


Figure 14 : CGY2139AUH/C1 Pad layout drawing

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on-wafer tested	30	-	4.5 x 4.1 x 0.1

SOLDERING

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330℃.

Temperature in excess of 300℃ should not be applie d to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400℃

ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2139A	UH	C1	-	On-Wafer measured Die

RoHS Compliant

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
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