

# PRELIMINARY DATASHEET

## CGY2170XUH/C2

### 6-bit X-Band Core Chip

#### DESCRIPTION

The CGY2170XUH is a high performance GaAs MMIC T/R 6-bit Core Chip operating in X-band. It includes a 6-bit phase shifter, a 6-bit attenuator, and switches. It has a phase shifting range of 360° and a gain setting range of 32 dB. It covers the frequency range from 8 to 12 GHz and can be used in Radar, Telecommunication and Instrumentation applications.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using OMMIC's 0.18  $\mu\text{m}$  gate length PHEMT Technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

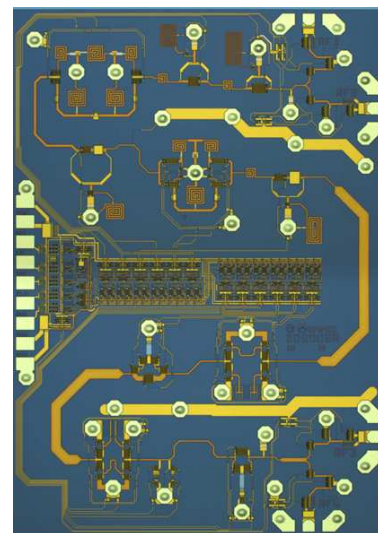
#### APPLICATIONS

- ▶ Radar
- ▶ Telecommunication
- ▶ Instrumentation



#### FEATURES

- ▶ Operating Range : 8 GHz to 12 GHz
- ▶ Insertion Loss : 15 dB @ 10 GHz
- ▶ RMS Phase Error  $\approx 3.0^\circ$  @ 10 GHz
- ▶ RMS Amplitude Error  $\approx 0.3$  dB @ 10 GHz
- ▶ Input P1dB  $\approx +20$  dBm
- ▶  $S_{11}$  &  $S_{22} \approx -15$  dB @ 10 GHz (all states)
- ▶ Total Power Consumption  $\approx 40$  mW
- ▶ Chip size = 4000 x 2850  $\mu\text{m}$
- ▶ Tested, Inspected Known Good Die (KGD)
- ▶ Samples Available



Photograph of the CGY2170XUH

## LIMITING VALUES

$T_{amb} = 25\text{ °C}$  unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
$V_{DN}$	Positive supply voltage		-1	+5	V
$V_{SN}$	Negative supply voltage		-5	+1	V
$D_{IN}$ , CLK and LE	Digital data input		-1	+7	V
$P_{IN}$	Input power	At RF 1 and RF 2		+25	dBm
$T_j$	Junction temperature			+150	°C
$T_{stg}$	Storage temperature		-55	+150	°C

## OPERATING CONDITIONS

$T_{amb} = 25\text{ °C}$  unless otherwise noted

Symbol	Parameter	Conditions	MIN.	TYP,	MAX,	UNIT
$V_{DN}$	Positive supply voltage		2,5	3	3,5	V
$V_{SN}$	Negative supply voltage		-3,5	-3	-2,5	V
$I_{DN}$	Positive supply current			2		mA
$D_{IN}$ , CLK and LE	Digital data input		2,5	3	3,5	V

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient ( $T_a = 25\text{ °C}$ )	TBD	°C/W

## CHARACTERISTICS

T<sub>amb</sub> = 25 °C – Typical RF Performance are given at 10 GHz. Min and Max values are given for all the 8-12 GHz frequency band.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
<i>DC Supplies</i>						
V <sub>DN</sub>	Positive supply voltage		2.5	3	3.5	V
I <sub>DN</sub>	Positive supply current			2		mA
V <sub>SN</sub>	Negative supply voltage		-3.5	-3	-2.5	V
I <sub>SN</sub>	Negative supply current			12		mA
<i>RF Performance at 10 GHz unless otherwise specified</i>						
BW	Bandwidth		8		12	GHz
IL	Insertion Loss at reference state			15	18	dB
NF	Noise Figure at reference state			15	18	dB
S <sub>11</sub> , S <sub>22</sub>	Input reflection coefficients (all states)	RF 1 and RF 2		-15	-10	dB
S <sub>33</sub> , S <sub>44</sub>	Output reflection coefficients (all states)	RF 3 and RF 4		-15	-10	dB
ISO	Switch isolation	RF 2 to RF 1		40		dB
ATT <sub>Range</sub>	Attenuation range			31.5		dB
ATT <sub>error (RMS)</sub>	RMS Attenuation Error wrt the 64 Attenuation States & at Reference Phase State			0.3	0.5	dB
ATT <sub>variation (RMS)</sub>	RMS Attenuation variation wrt the 64 Phase States & at Reference Attenuation State			0.3	0.8	dB
PH <sub>Range</sub>	Phase range			-354		°
PH <sub>error (RMS)</sub>	RMS Phase Error wrt the 64 Phase States & at Reference Attenuation State			3	5	°
PH <sub>variation (RMS)</sub>	RMS Phase Variation wrt the 64 Attenuation States & at Reference Phase State			3	6	°
P <sub>1dB</sub>	Input 1dB compression point	No Attenuation	16	20		dBm
T <sub>switch</sub>	Switching time			100		ns
Rate	Serial data rate			20	> 230	Mbps

Note : The RMS value is the root mean square of the error defined as below :

$$x_{RMS} = \sqrt{\frac{1}{N} \sum_{i=1}^N x_i^2} = \sqrt{\bar{x}_i^2 + \sigma_{x_i}^2}$$

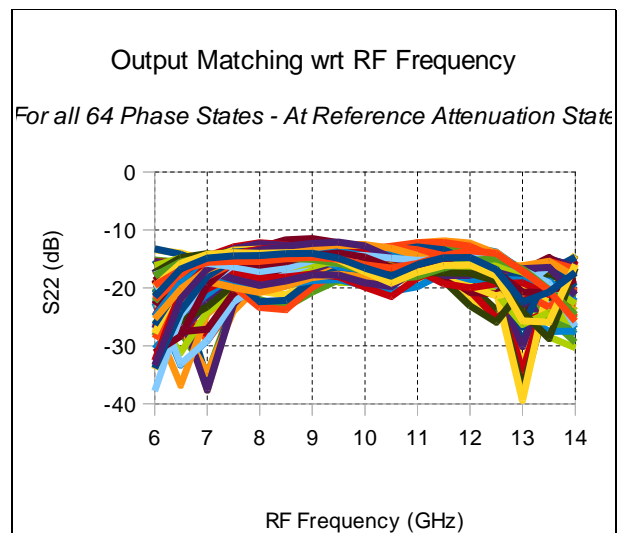
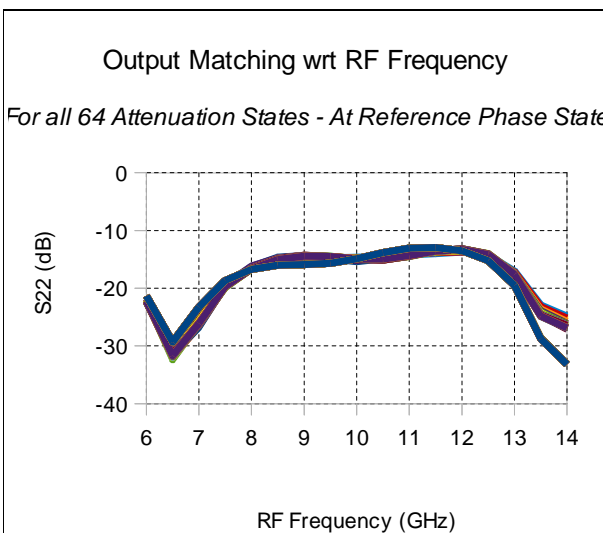
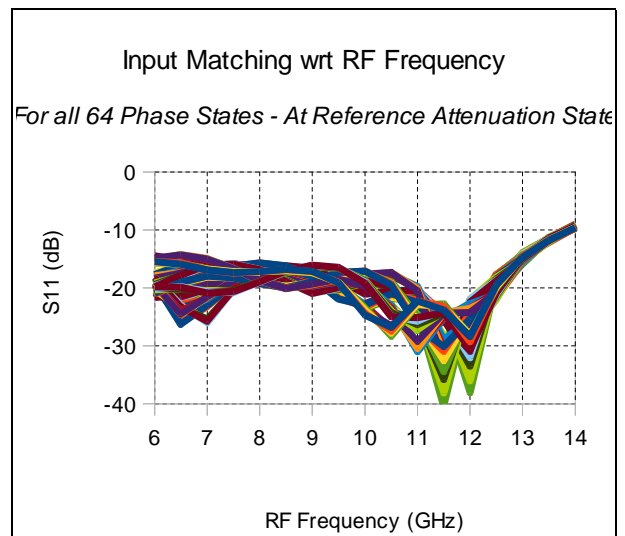
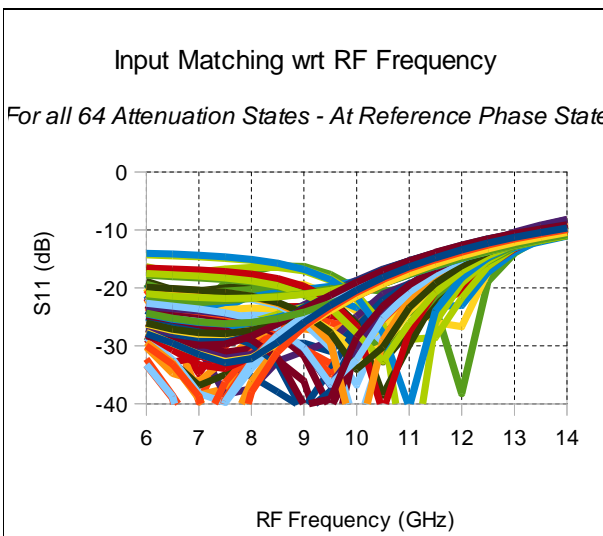
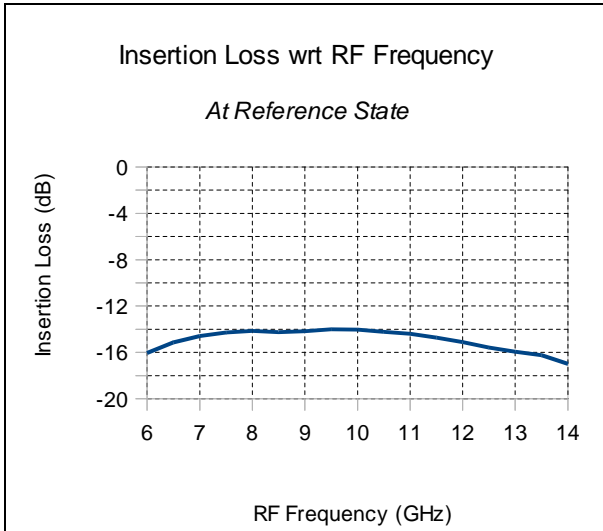
Where x<sub>i</sub> is the difference between the measured value and the theoretical value,  $\bar{x}_i$  is the mean value of the N x<sub>i</sub>, and σ<sub>x<sub>i</sub></sub> is the standard deviation of x<sub>i</sub>.



**Caution** : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

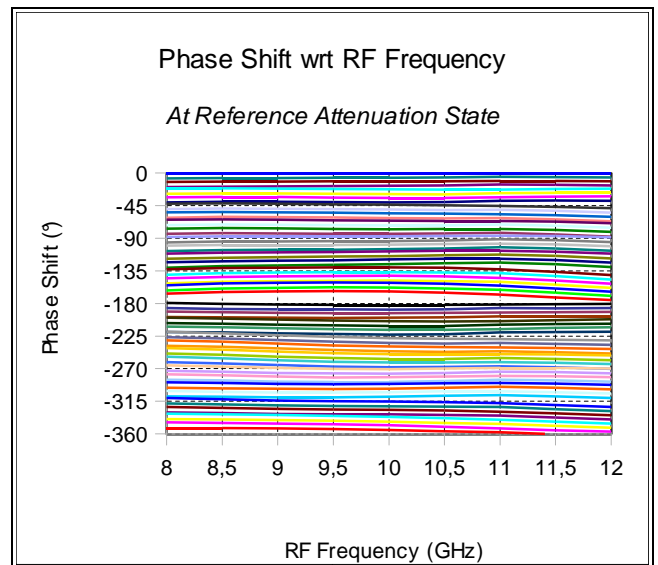
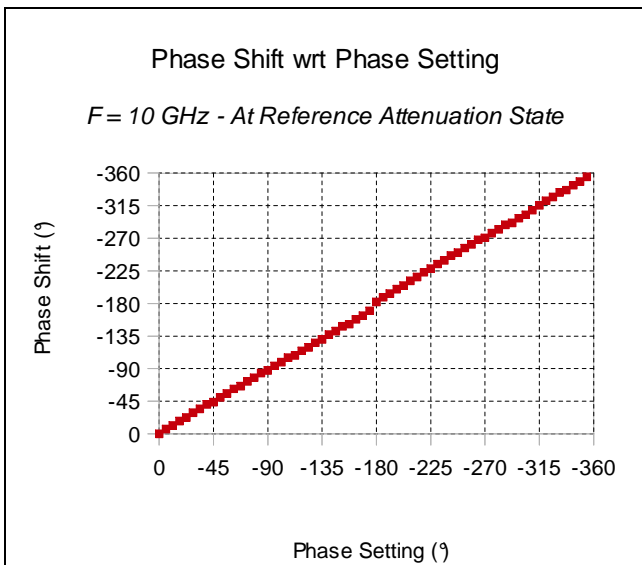
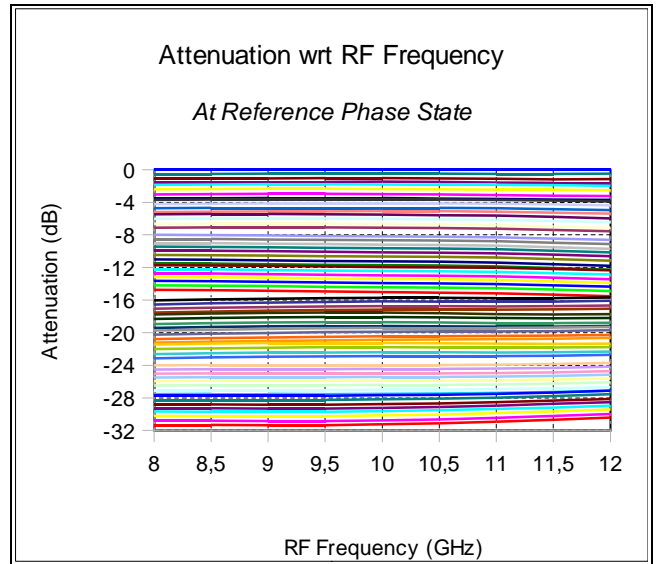
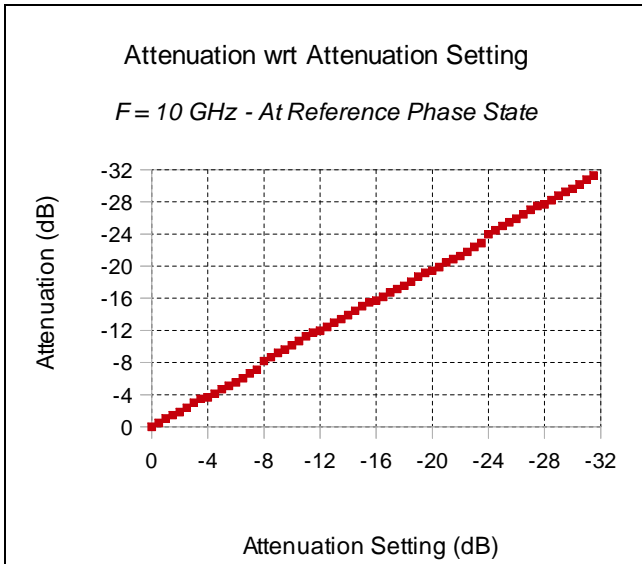
**ON WAFER MEASUREMENTS – S PARAMETERS**

Measured on Input ports at nominal power supply voltages and at T = 25 °C.  
 Calculated with input and output inductance of 0.3 nH to take into account the bonding inductance.



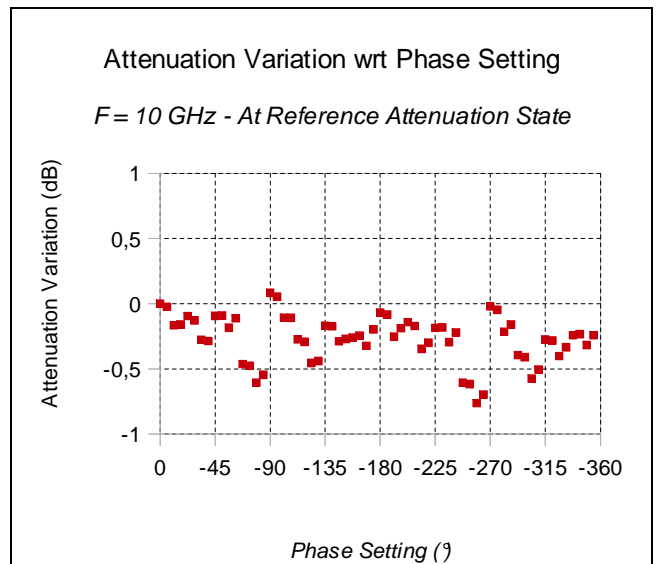
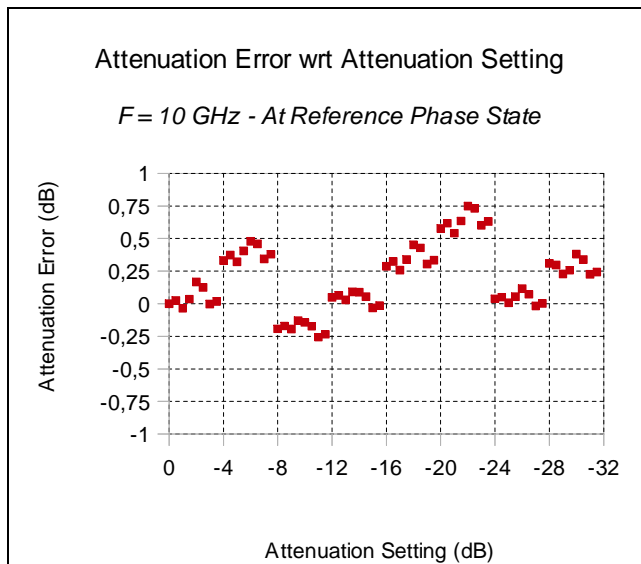
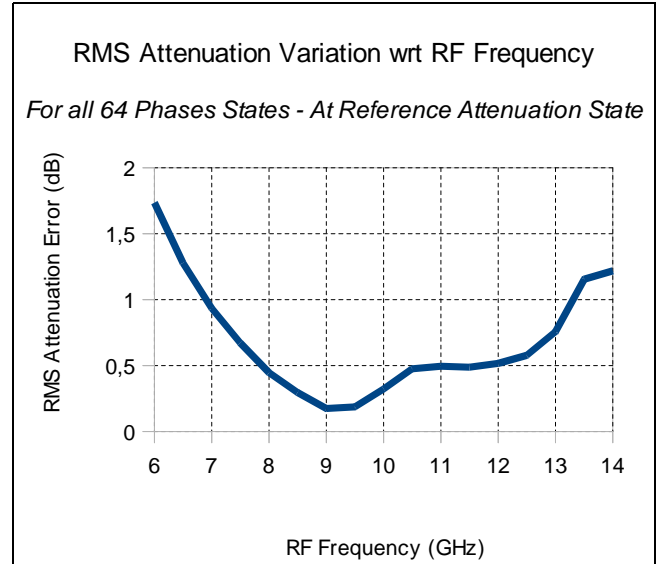
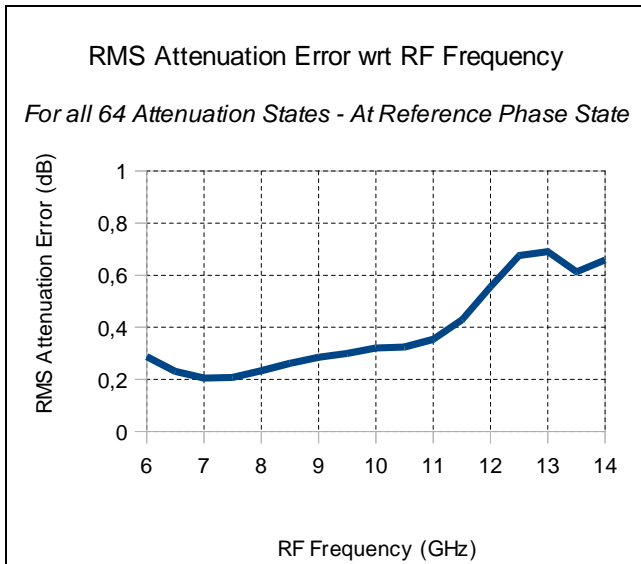
**ON WAFER MEASUREMENTS – ATTENUATOR & PHASE SHIFTER RESPONSE**

Measured on Input ports at nominal power supply voltages and at T = 25 °C.  
Calculated with input and output inductance of 0.3 nH to take into account the bonding inductance.



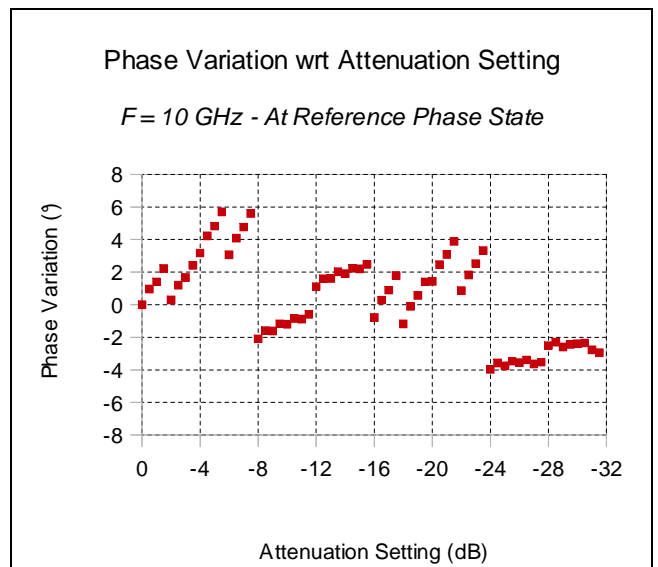
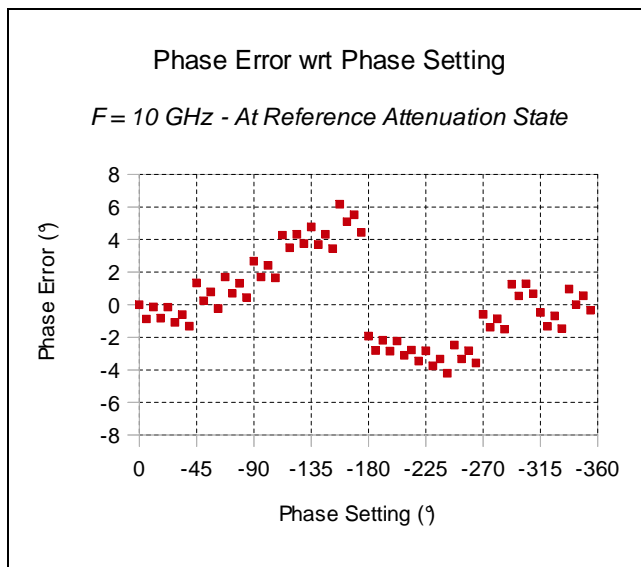
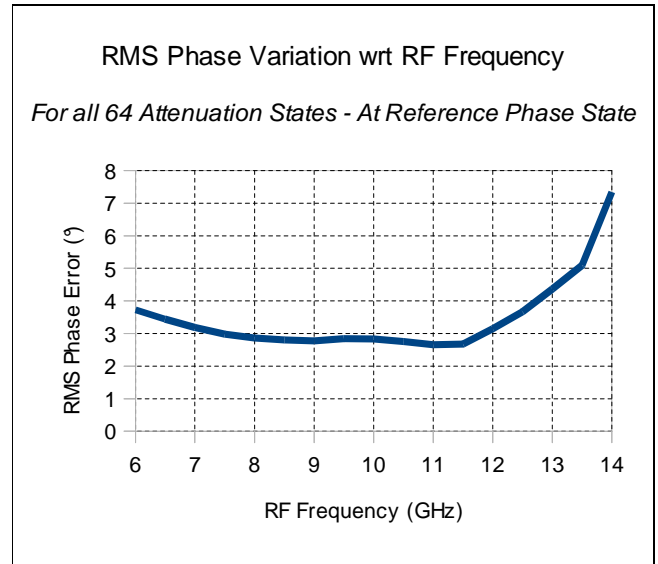
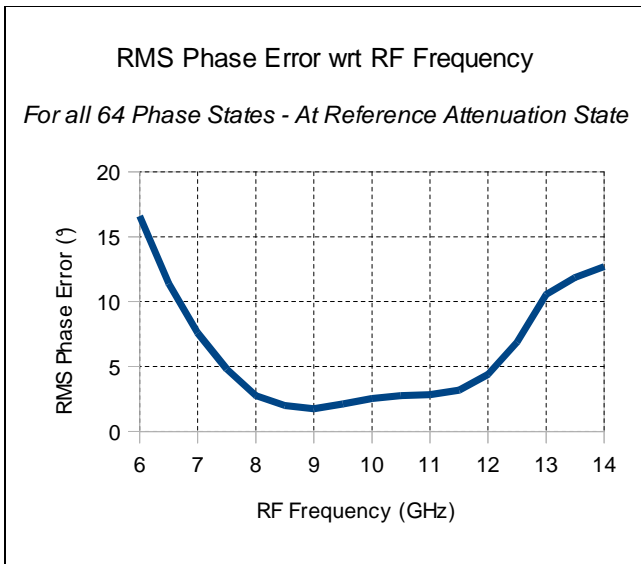
## ON WAFER MEASUREMENTS – ATTENUATION ERRORS

Measured on Input ports at nominal power supply voltages and at T = 25 °C.  
Calculated with input and output inductance of 0.3 nH to take into account the bonding inductance.



**ON WAFER MEASUREMENTS – PHASE SHIFTING ERRORS**

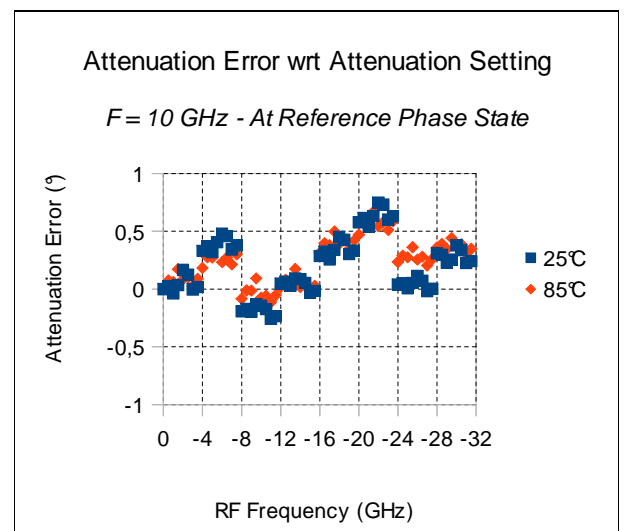
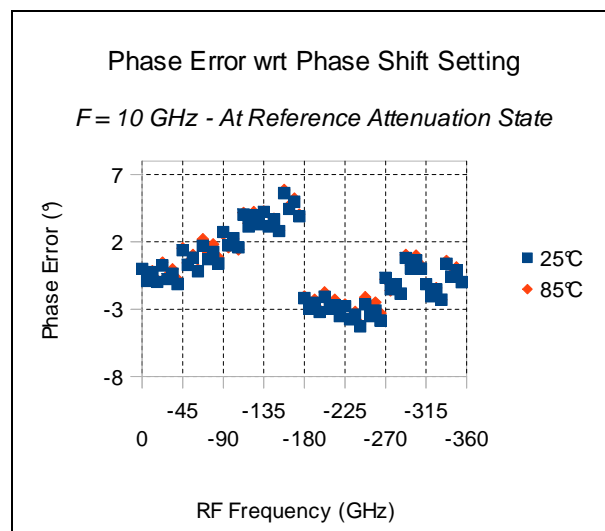
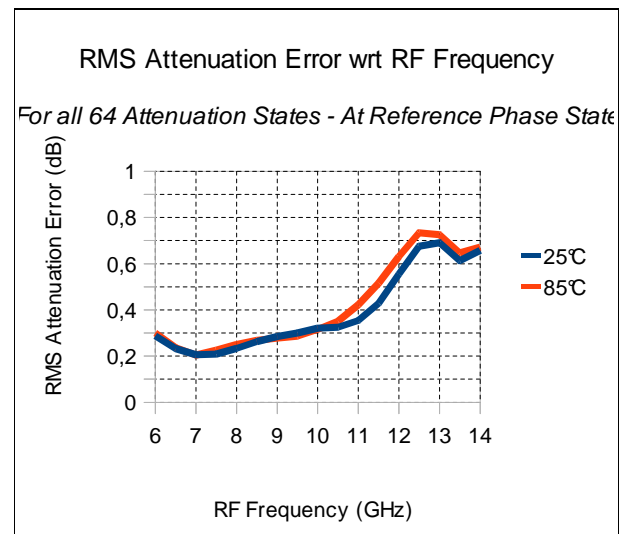
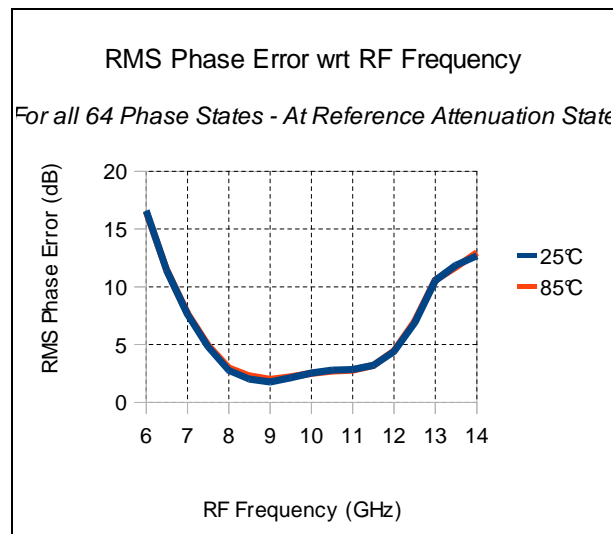
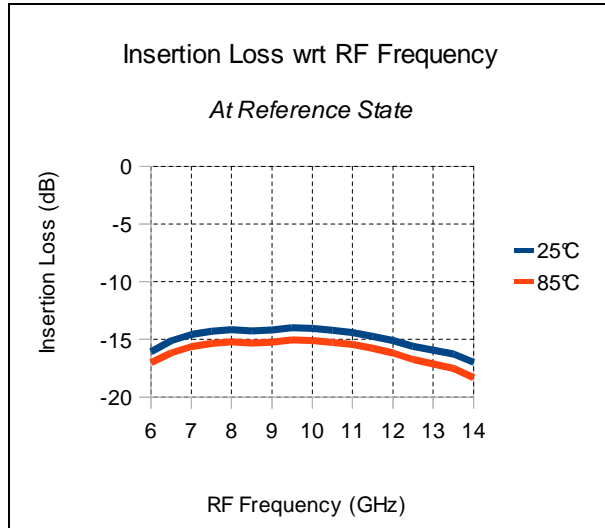
Measured on Input ports at nominal power supply voltages and at T = 25 °C.  
 Calculated with input and output inductance of 0.3 nH to take into account the bonding inductance.



## ON WAFER MEASUREMENTS – HIGH TEMPERATURE MEASUREMENTS

Measured on Input ports at nominal power supply voltages and at  $T = 85\text{ }^{\circ}\text{C}$ .

Calculated with input and output inductance of 0.3 nH to take into account the bonding inductance.





**DATA**

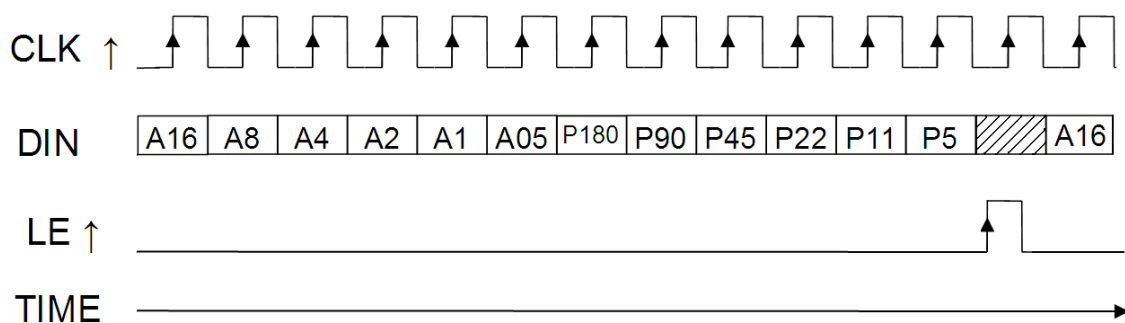
Bit Number	Description	Reference State	Theoretical Value
B0	Attenuator A16	High	16 dB
B1	Attenuator A8	High	8 dB
B2	Attenuator A4	High	4 dB
B3	Attenuator A2	High	2 dB
B4	Attenuator A1	High	1 dB
B5	Attenuator A05	High	0.5 dB
B6	Phase shifter P180	High	-180°
B7	Phase shifter P90	High	-90°
B8	Phase shifter P45	High	-45°
B9	Phase shifter P22	High	-22.5°
B10	Phase shifter P11	High	-11.25°
B11	Phase shifter P5	High	-5.625°

**CONTROL VOLTAGE (CMOS STANDARD LOGIC)**

State	Vmin	Vmax
Low	0 V	1 V
High	+2.5 V	V <sub>DN</sub>

**TIME DIAGRAM**

- DATA\_IN is sampled at the rising edge of CLK.
- Rising Edge of LE must occur when all the 12 bits are loaded and on low level of CLK.
- DATA IN is transferred and Attenuator / Phase Shifter positions changed on high level of LE.

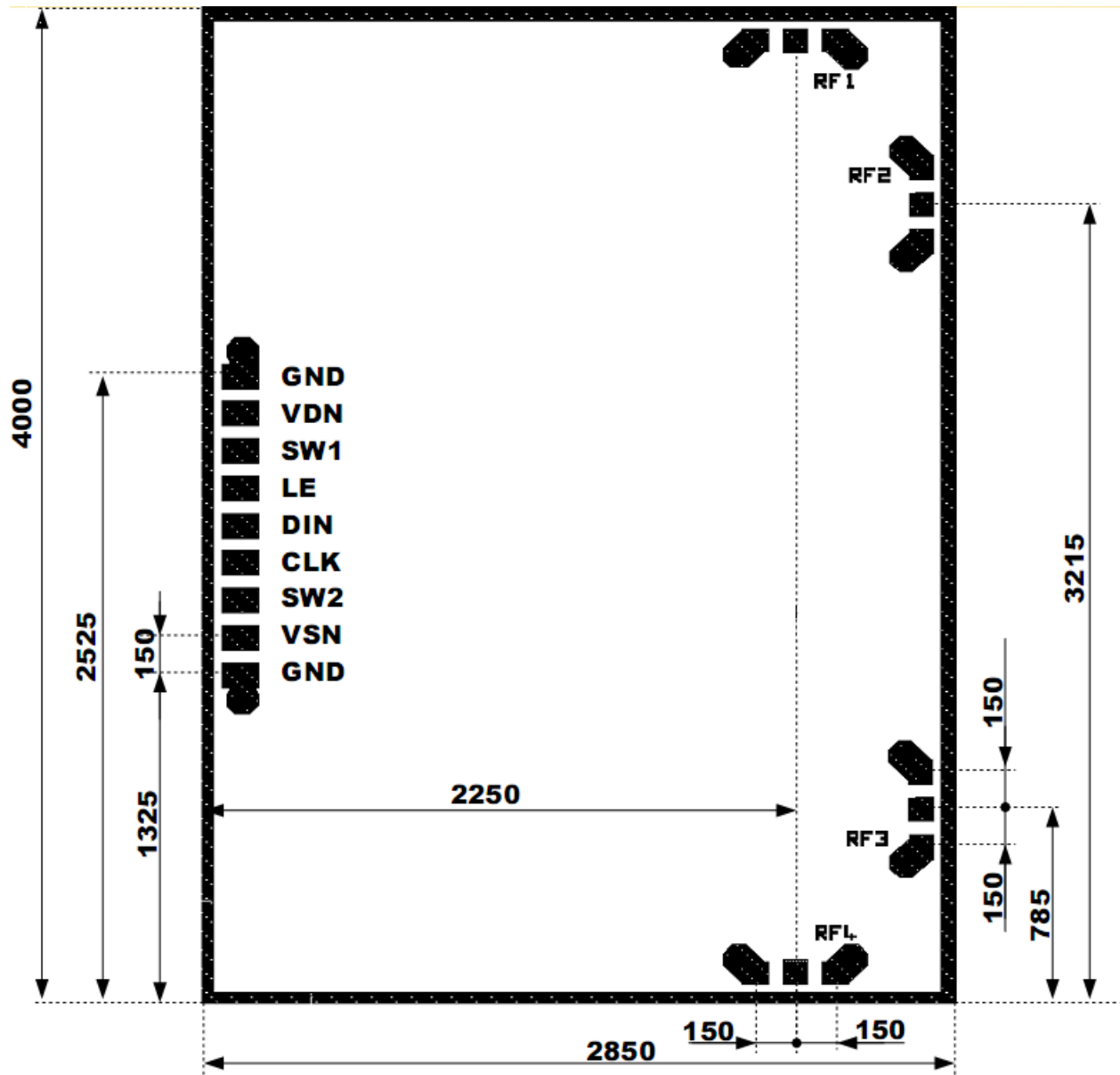

**SWITCHES CONTROL**

	Switch 1	Switch 2
Low (0V)	RF1	RF3
High (3V)	RF2	RF4

## MECHANICAL INFORMATION

Chip size = 4000 x 2850  $\mu\text{m}$  (before wafer sawing)

- DC Pads = 100 x 140  $\mu\text{m}$ , spacing = 150  $\mu\text{m}$ , top metal=Au
- RF Pads = 95 x 95  $\mu\text{m}$ , pitch = 150  $\mu\text{m}$ , top metal=Au
- Chip Thickness 100  $\mu\text{m}$



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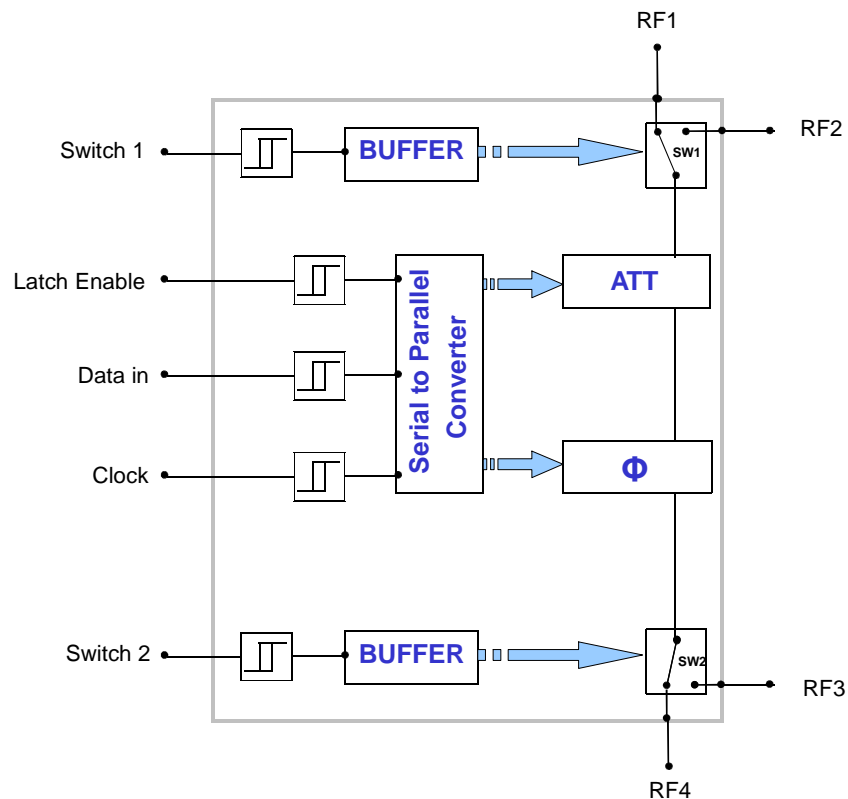
## PAD POSITION

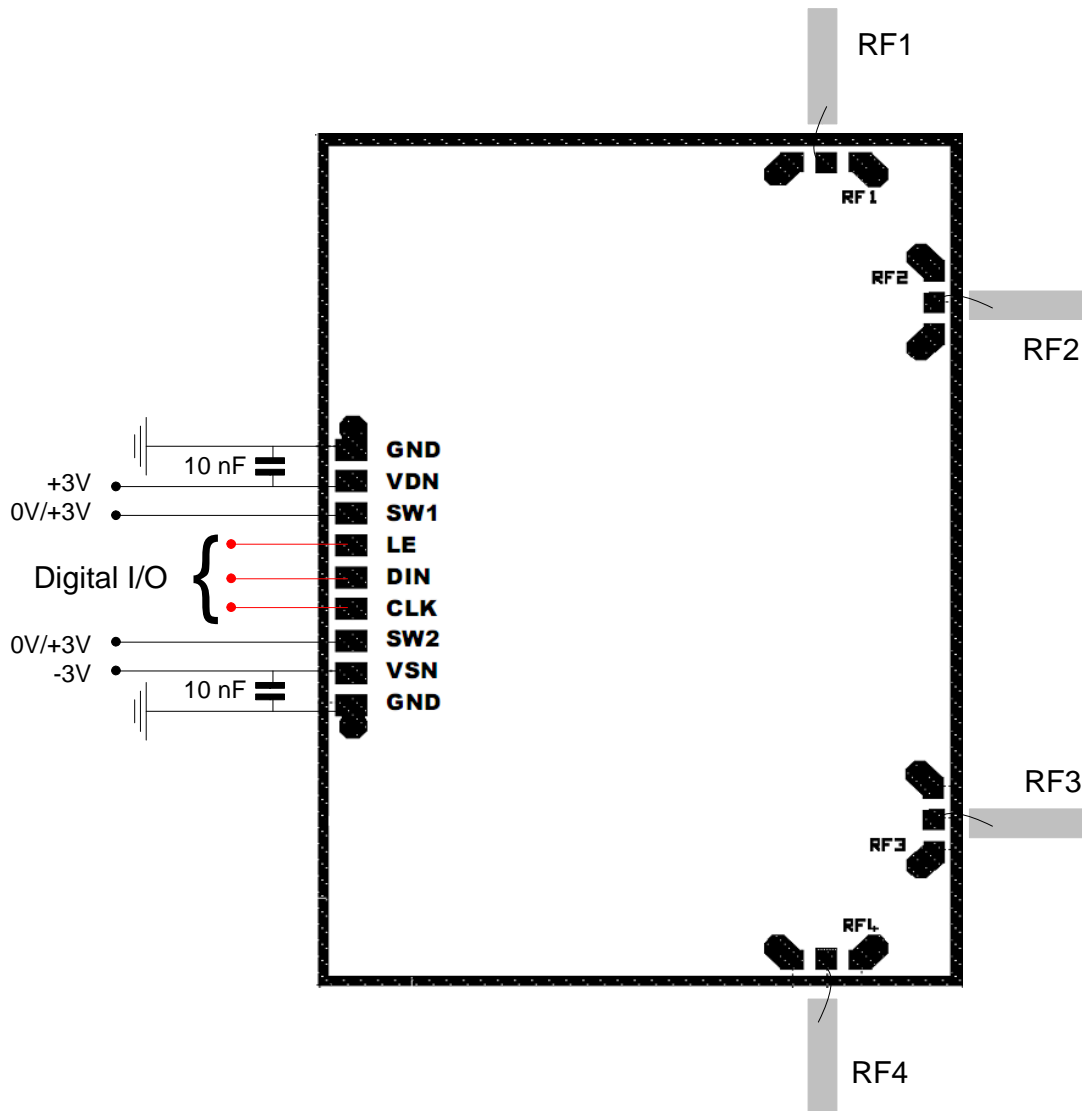
SYMBOL	COORDINATES		DESCRIPTION
	X	Y	
GND	120	2525	Ground
VDN	120	2375	Positive Control Voltage
SW1	120	2225	Switch 1 Control Voltage
LE	120	2075	Latch Enable Input
DIN	120	1925	Data Input
CLK	120	1775	Clock Input
SW2	120	1625	Switch 2 Control Voltage
VSN	120	1475	Negative Control Voltage
GND	120	1325	Ground
RF1	2250	3900	RF Input Port 1
RF2	2750	785	RF Input Port 2
RF3	2750	3215	RF Output Port 3
RF4	2250	100	RF Output Port 4

X=0, Y=0 at bottom left corner.

See Mechanical Information for more details.

## BLOCK DIAGRAM



**BONDING DIAGRAM AND ASSEMBLY INFORMATION**


The RF interfacing bond wires or ribbon should be kept as short as possible. The RF lines should be 300  $\mu\text{m}$  wide or less to minimize discontinuities associated with the connection to the MMIC Bond pads.



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**DEFINITIONS**
**Limiting values definition**

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information**

Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**DISCLAIMERS**
**Life support applications**

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**Right to make changes**

OMMIC reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. OMMIC assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

**ORDERING INFORMATION**

Generic type	Package type	Version	Sort Type	Description
CGY2170XUH	Bare Die	C2		6-bit X-band Core Chip


**Document History : Version 1.2, Last Update 19/09/2011**