PRODUCT DATASHEET

CGY2175AUH/C1

3-Port C-Band Integrated Core Chip

DESCRIPTION

The CGY2175AUH is a high performance GaAs MMIC 3 port, 6–bit Core Chip operating in C-band. It includes a 6-bit phase shifter, a 6-bit attenuator and T/R switch. The on-chip Series to Parallel Converter minimizes the number of bonding pads and greatly simplifies the use of the Core Chip functions.

The die is manufactured using OMMIC's 0.18 µm gate length PHEMT Technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

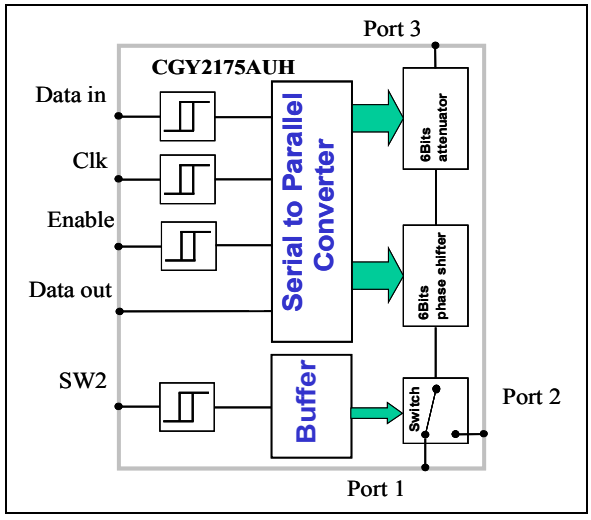
This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

FEATURES

- Operating Range : 4.5 GHz to 6.5 GHz
- Insertion Loss : 12 dB @ 5.4 GHz
- Phase Shift Range = 360°
- Attenuation Range = 31.5 dB
- RMS Phase Error ≈ 1.3° @ 5.4 GHz
- RMS Amplitude Variation ≈ 0.2 dB @ 5.4 GHz
- S_{11} & S_{22} < -14 dB @ 5.4 GHz (All states)
- Total Power Consumption ≈ 0.1 W
- Chip size = 3765 x 4465 µm ± 5 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD Available

APPLICATIONS

- Radar
- Telecommunication
- Instrumentation



Block diagram of the 6 bit C-band Core Chip

RoHS Compliant

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LIMITING VALUES

T_{amb} = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_d	Positive supply voltage (Schmidt trigger)		-5	+7	V
V_{c1}	Negative supply voltage (Schmidt trigger)		-5	+5	V
V_{c2}	Negative supply voltage (Digital)		-5	+5	V
D_{IN},CLK and LE	Digital data input		-5	+7	V
P_{IN}	Input power	At RF Port 1 and Port 2		+25	dBm
T_{amb}	Ambient temperature		-40	+85	° C
T_j	Junction temperature			+150	° C
T_{stg}	Storage temperature		-55	+150	° C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j-a)}$	Thermal resistance from junction to ambient (T_a = 25 °C)	TBD	° C/W

CHARACTERISTICS

T_{amb} = 25 °C – RF Performance measured on wafer.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Supplies						
V_d	Positive supply voltage (Schmidt trigger)		4.5	5	5.5	V
I_d	Positive supply current (Schmidt trigger)			9		mA
V_{c1}	Negative supply voltage (Schmidt trigger)		-3.25	-3	-2.75	V
I_{c1}	Negative supply current (Schmidt trigger)			10		mA
V_{c2}	Negative voltage (digital)		-3.25	-3	-2.75	V
I_{c2}	Negative current (digital)			9		mA
RF Performance at 5.4 GHz unless otherwise specified						
BW	Bandwidth		4.5		6.5	GHz
IL	Insertion Loss at reference state	No Attenuation		11.7		dB
S_{11} , S_{22}	Input reflection coefficients	Port 1 and Port 2		-14		dB
S_{33}	Output reflection coefficient	Port 3		-14		dB
S_{13}	Attenuation	Port 3 to Port 1		-11.7		dB
S_{23}	Attenuation	Port 3 to Port 2		-11.7		dB
ISO	Switch isolation	Port 2 to Port 1	-40			dB
ATT_{range}	Attenuation range			31.5		dB
$ATT_{error\ (rms)}$	RMS Attenuation error (see note 1) versus attenuator setting			0.18		dB
$ATT_{variation\ (max)}$	Attenuation variation with phase setting (max)		-0.2		+0.7	dB
PH_{range}	Phase range			360		°
$PH_{error\ (rms)}$	RMS Phase error (see note 1) versus phase shifter setting			1.25	4	°
$PH_{variation\ (max)}$	Phase variation with attenuation setting (max) (see note1)		-3		+3	°
$P_{1dB\ (TX)}$	Input 1 dB compression point (TX)	No Attenuation		+20		dBm
T_{switch}	Switching time Rx/Tx			10		ns
Rate	Serial data rate			100		MHz

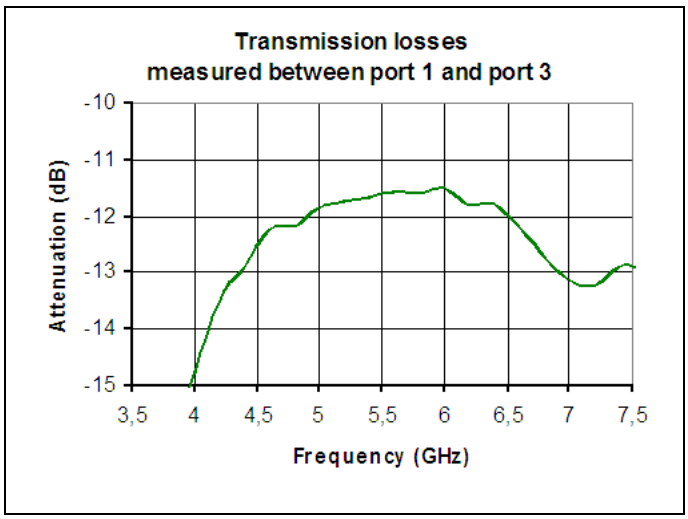
Note1 : The RMS value is the root mean square of the error defined as below

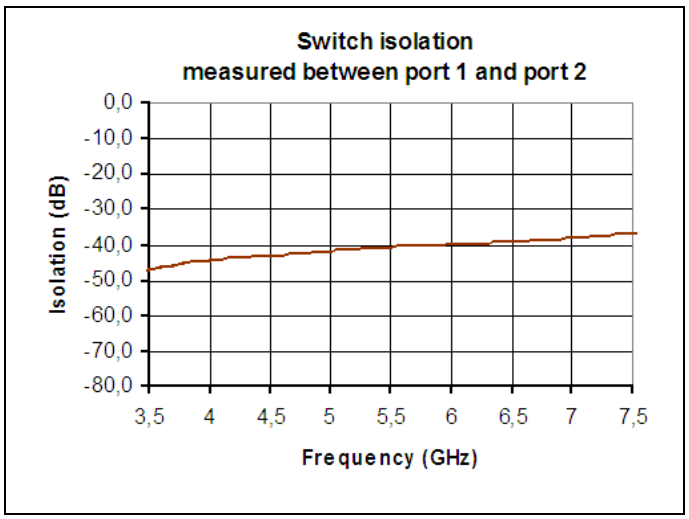
$$x_{\mathrm{rms}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \cdots + x_N^2}{N}}$$

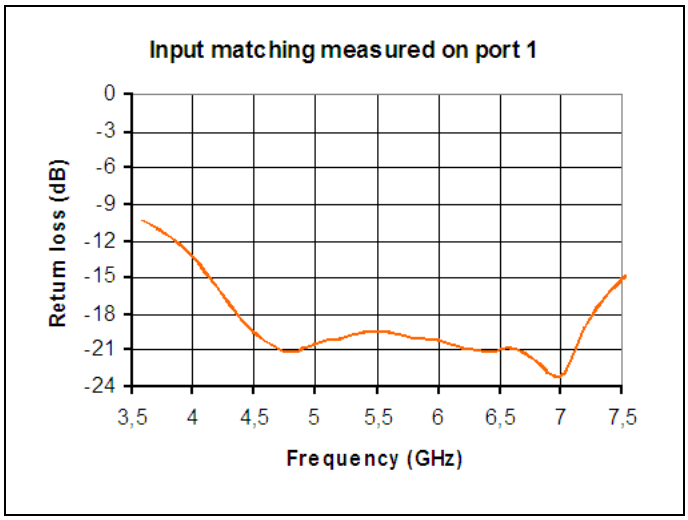
Where x_i is the difference between the measured value and the expected value.

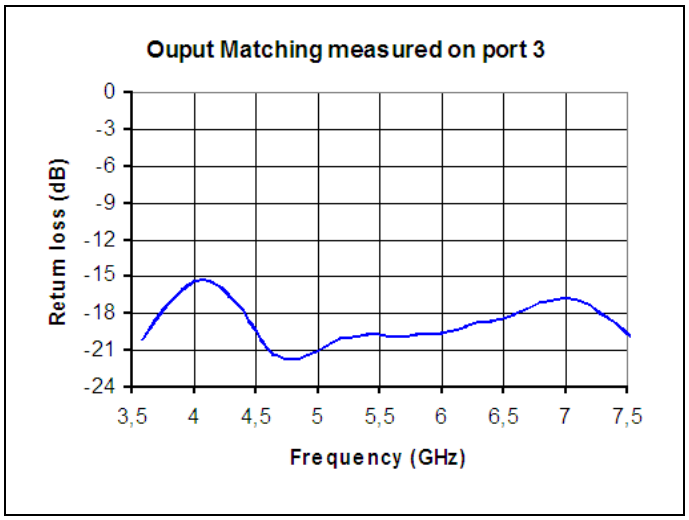
ON WAFER MEASUREMENTS – S PARAMETERS

Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V



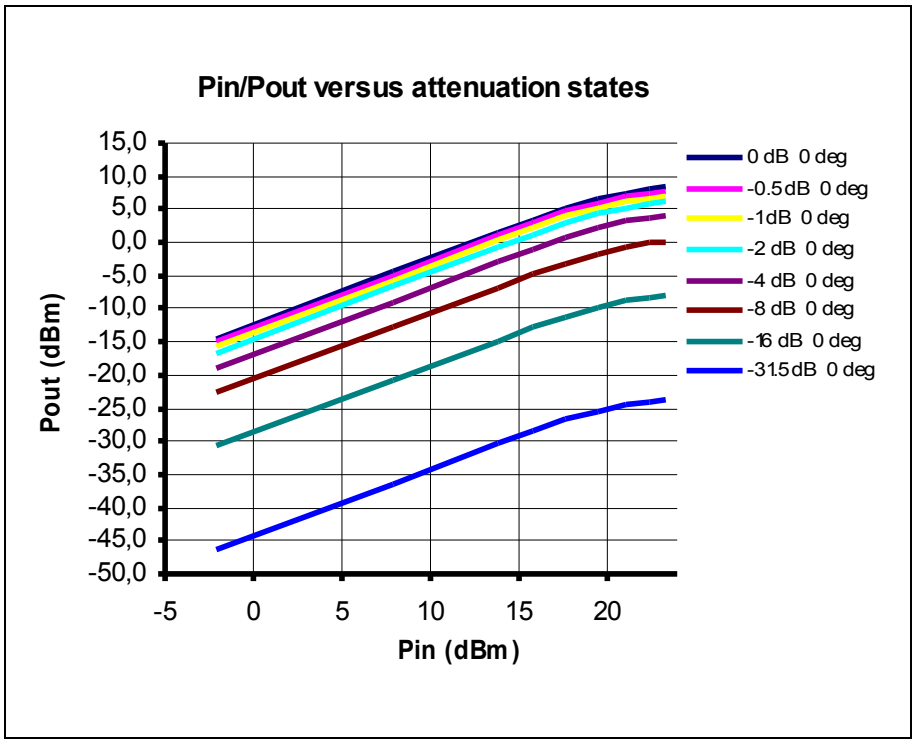


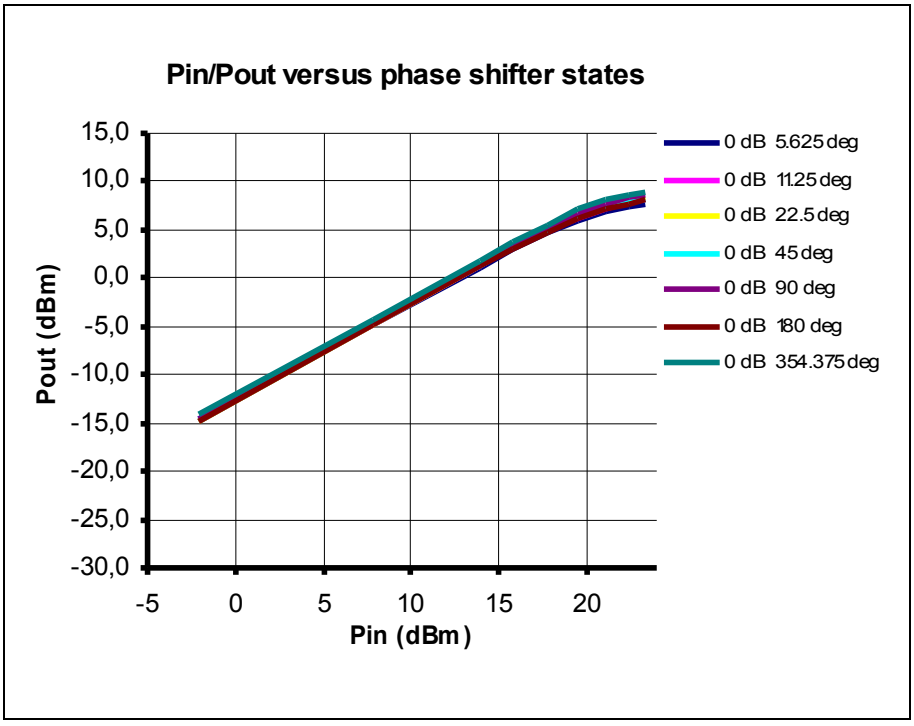




ON WAFER MEASUREMENTS – 1 dB COMPRESSION POINT

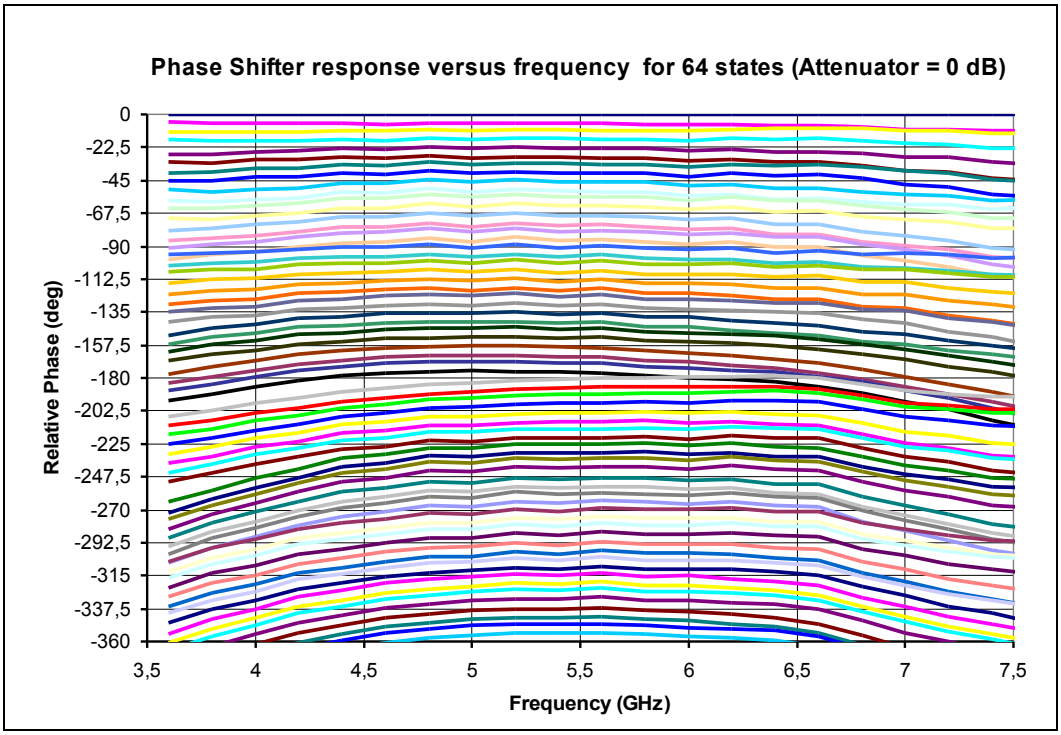
Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V

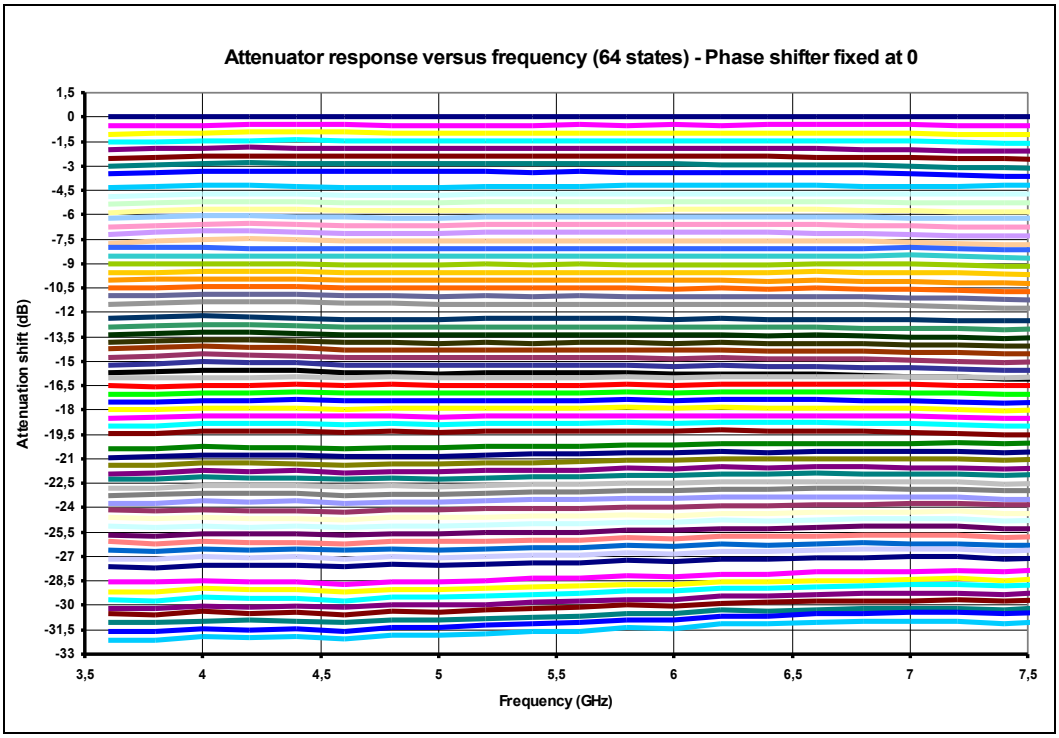




ON WAFER MEASUREMENTS – ATTENUATOR & PHASE SHIFTER RESPONSE

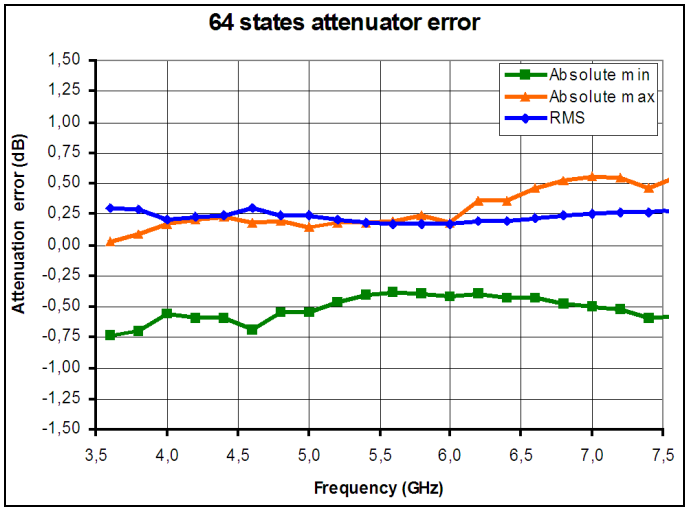
Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V

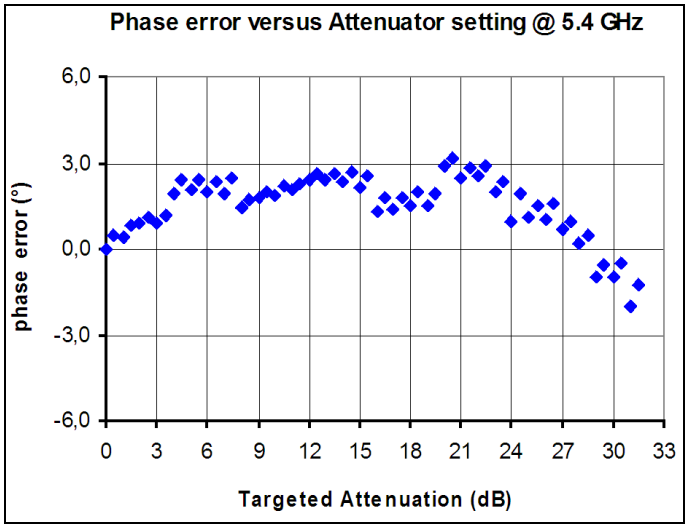


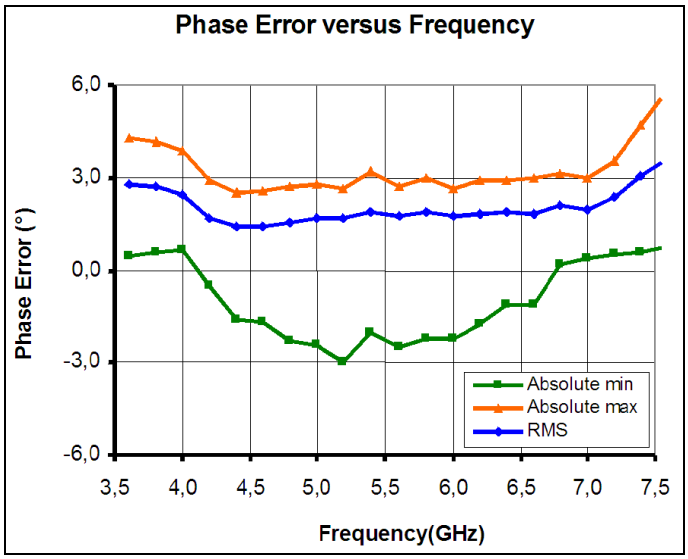


ON WAFER MEASUREMENTS – ATTENUATOR ERRORS

Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V

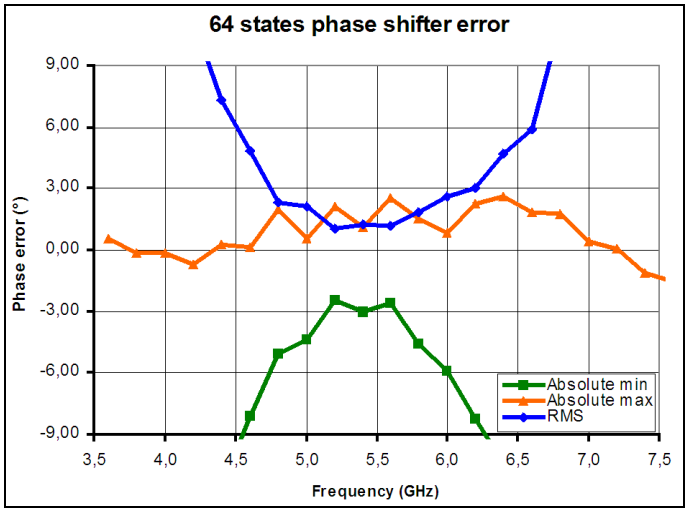


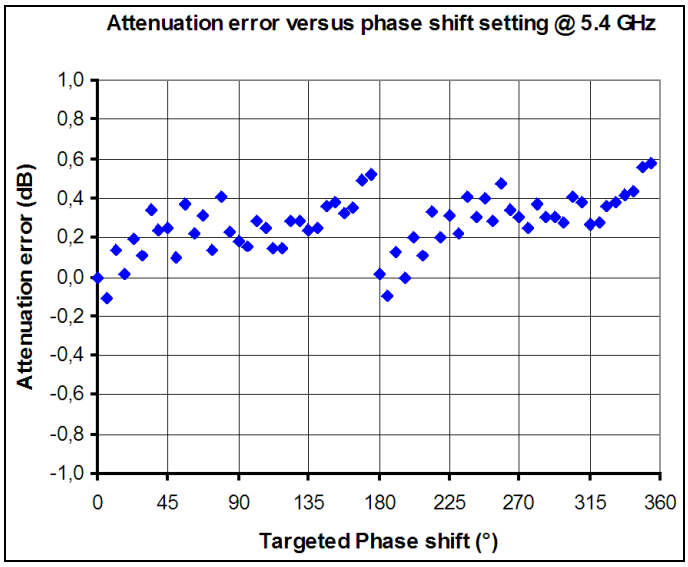


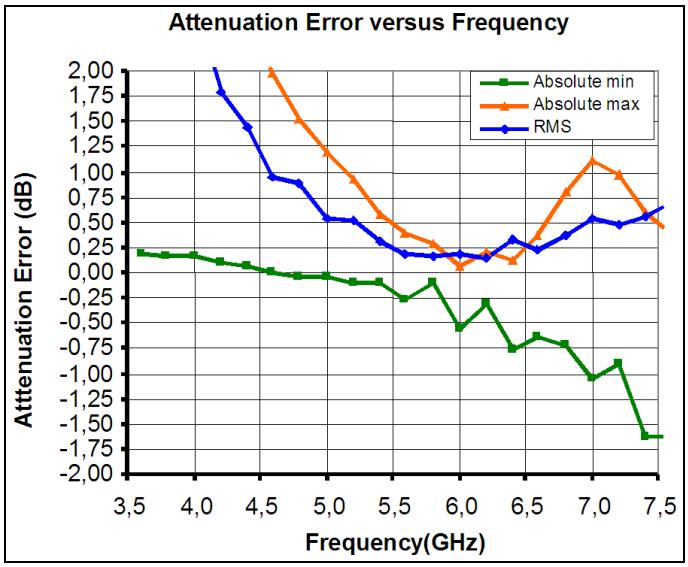


ON WAFER MEASUREMENTS – PHASE SHIFTER ERRORS

Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V

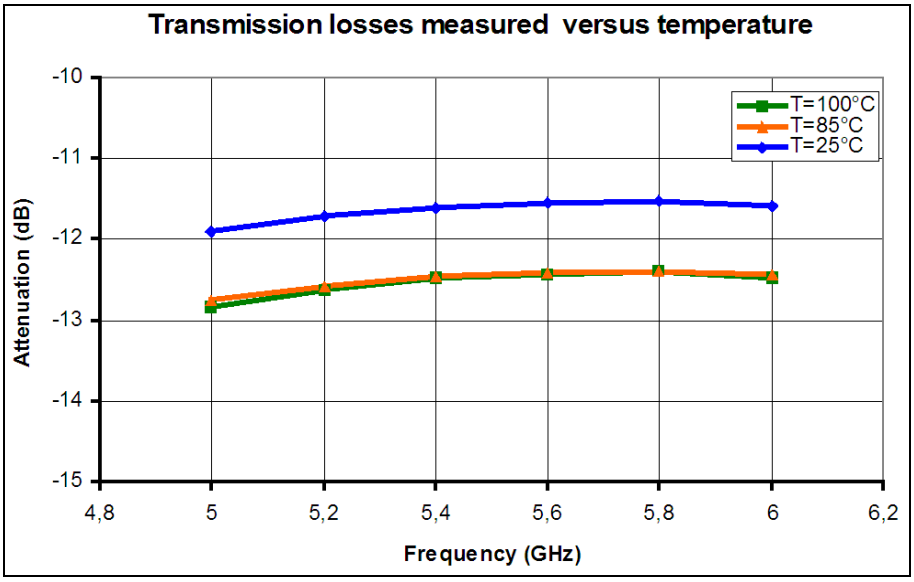


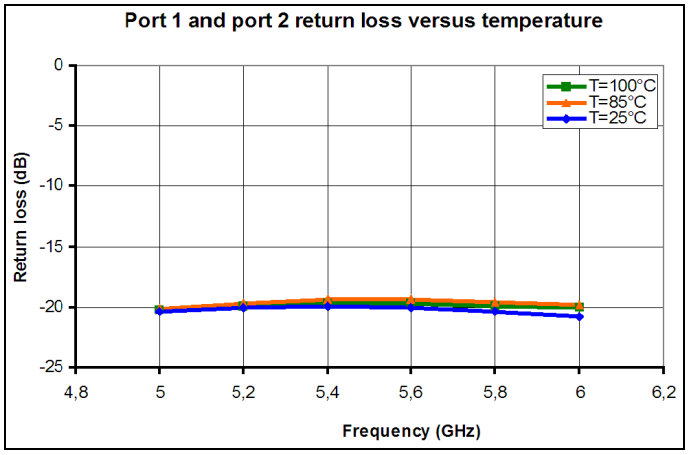


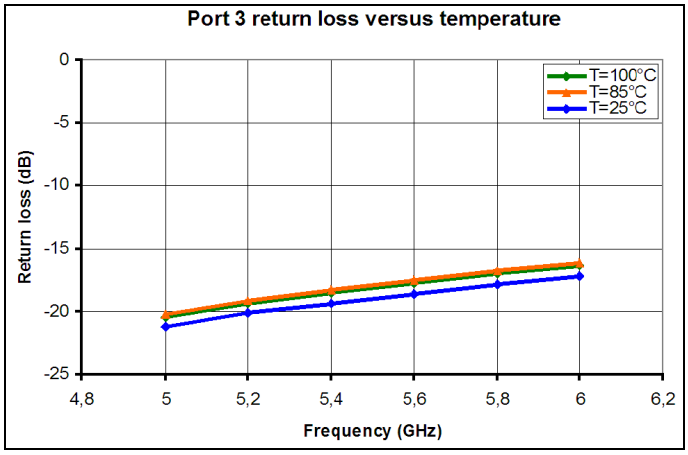


ON WAFER MEASUREMENTS – REFERENCE STATE VERSUS TEMPERATURE

Measured on reference state @ T = 25 °C ; V_{dd} = 5 V ; V_{cc1} = V_{cc2} = -3 V; SW2 = +5 V







LOGIC TRUTH TABLE

Control register bits assignments : B0 is loaded first and B11 last, see timing diagram.

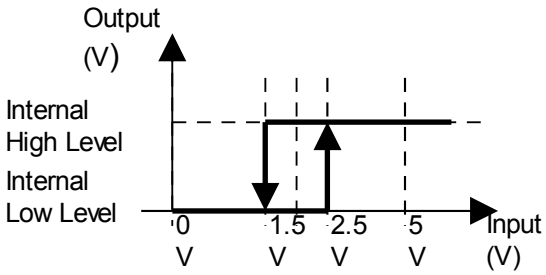
Bit	Description	Reference state	Value
DATA - B0(LSB ph)	Phase shifter B0	High	5.625°
DATA - B1	Phase shifter B1	High	11.25°
DATA - B2	Phase shifter B2	High	22.5°
DATA - B3	Phase shifter B3	High	45°
DATA - B4	Phase shifter B4	High	90°
DATA - B5	Phase shifter B5	High	180°
DATA - B6(LSB att)	Attenuator B0	High	0.5 dB
DATA - B7	Attenuator B1	High	1 dB
DATA - B8	Attenuator B2	High	2 dB
DATA - B9	Attenuator B3	High	4 dB
DATA - B10	Attenuator B4	High	8 dB
DATA - B11	Attenuator B5	High	16 dB
CLK	Clock	-	-
LE	Latch Enable	-	-
SW1	Not Used	Connected to ground	-
SW2	Port 1 ←→ Port 2 Switch	High	RF path between Port 1 and Port 3 Port 2 isolated and loaded by 50 Ω
		Low	RF path between Port 2 and Port 3 Port 1 isolated and loaded by 50 Ω

CONTROL VOLTAGE (CMOS STANDARD LOGIC)

State	MIN.	MAX.	UNIT
Low	0	0.3 x V_{dd}	V
High	0.5 x V_{dd}	V_{dd}	V

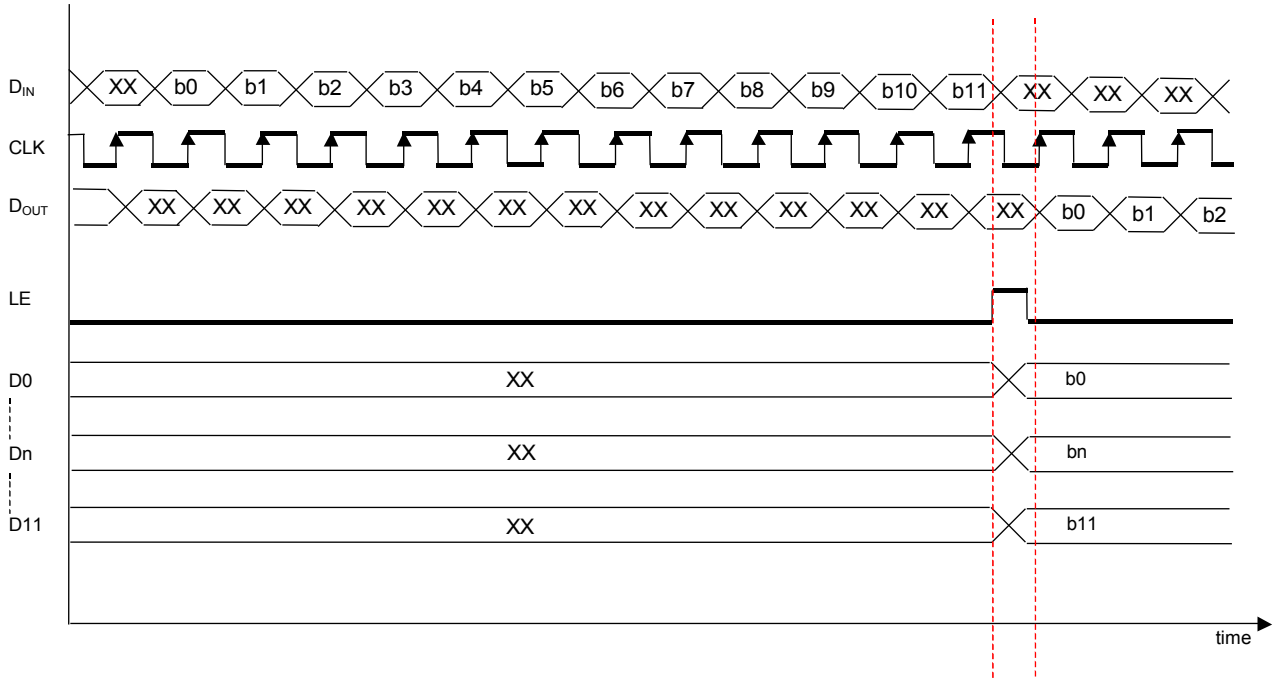
INPUT SCHMIDT TRIGGER

All inputs (DATA (D_{IN}), Clock (CLK), Latch Enable (LE) and Switch Control (SW2)) include Schmidt triggers allowing an optimal data transfer to the CGY2175AUH even in a noisy environment and/or high speed data stream.



TIMING DIAGRAM

- DATA (D_{IN}) is sampled at the rising edge of the Clock (CLK).
- Latch Enable (LE) must occur after all the 12 bits are loaded (i.e. after the rising edge associated with the bit b11) but before the subsequent rising edge of the Clock.
- The transferred data (D_{OUT}) is available on the rising edge of the Clock following the Latch enable.

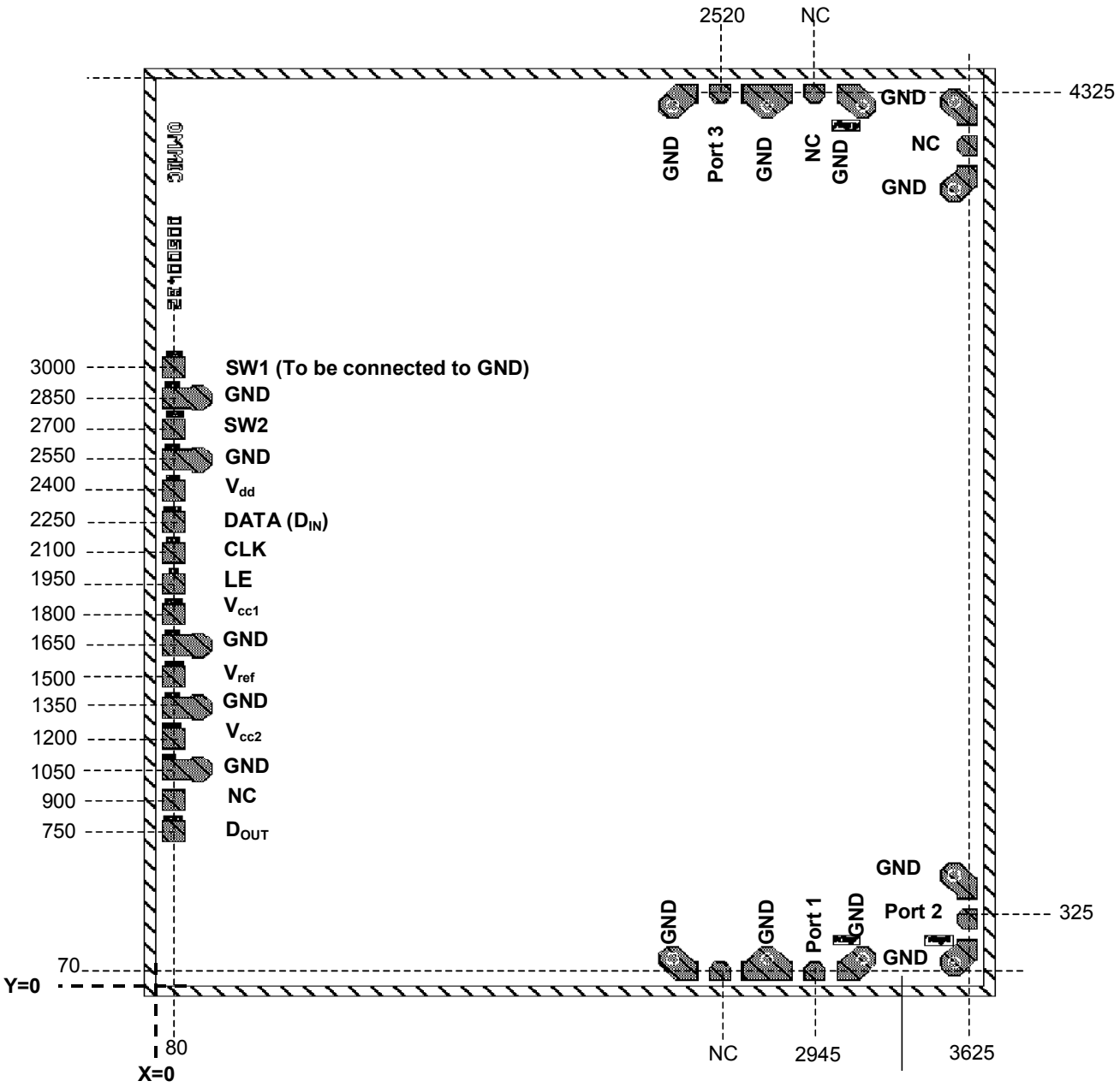


D_{IN} is the serial word containing 12 bits of information b0 to b11. Bits D0 to D11 are the internal parallel data used for the digital attenuator and digital phase shifter settings and is formed from the serial word b0 to b11.

MECHANICAL INFORMATION

Chip size = 3765 x 4465 µm (± 5 µm) including the dicing street

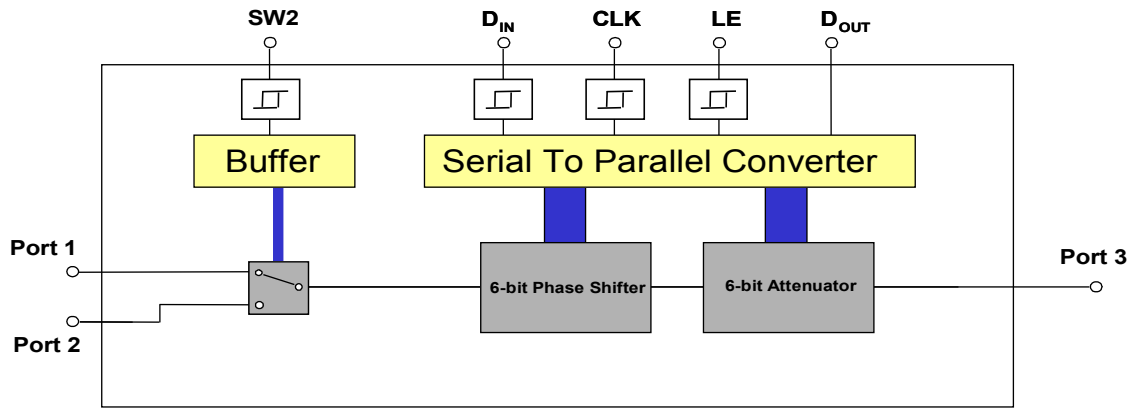
- DC Pads = 100 x 100 µm, spacing = 150 µm, top metal = Au
- RF Pads = 100 x 100 µm, spacing = 150 µm, top metal = Au
- Chip Thickness 100 µm



NC : Not connected

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

BLOCK DIAGRAM AND PAD CONFIGURATION



Block Diagram of the CGY2175AUH fully Integrated C-band 3-port T/R chip

PAD POSITION

PAD NAME	SYMBOL	COORDINATES		DESCRIPTION
		X	Y	
SW1	SW1	80	3000	Not used – Must be connected to ground
SW2	SW2	80	2700	Tx/Rx mode switch command
DATA (DIN)	D_{IN}	80	2250	Serial data input
CLK	CLK	80	2100	Clock for serial to parallel converter
LE	LE	80	1950	Latch Enable command to load the data
DOUT	D_{OUT}	80	750	Serial to parallel converter output for testing or to chain several chips
Vdd	V_d	80	2400	Schmidt trigger positive supply voltage (+5 V)
Vcc1	V_{c1}	80	1800	Schmidt trigger negative supply voltage (-3 V)
Vcc2	V_{c2}	80	1200	Serial to parallel converter negative supply voltage (-3 V)
Vref	V_{ref}	80	1500	Internal voltage supply for Converter – Must be decoupled using 100 nF Nominal value = -2 V
Port 1	Port 1	2945	70	RF Input/Output
Port 2	Port 2	3625	326	RF Input/Output
Port 3	Port 3	2520	4325	RF Input/Output

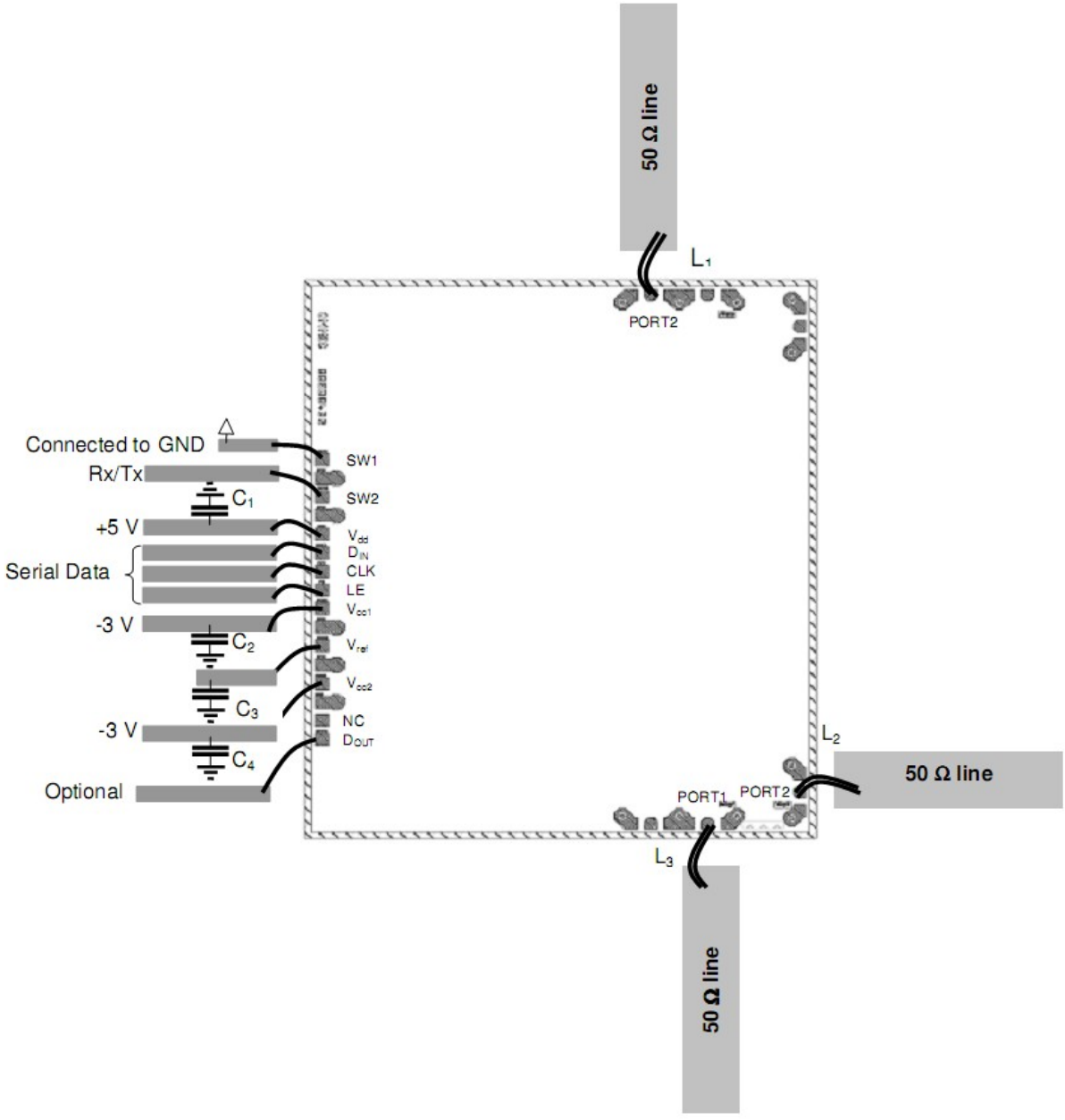
X=0, Y=0 at bottom left corner.
See Mechanical Information for more details.

BONDING DIAGRAM AND ASSEMBLY INFORMATION

The number of Wire Bonds to the RF pads (L_1, L_2, L_3) may be doubled to reduce the equivalent inductance. The optimal inductance is 0.35 nH in order to achieve the best return loss in the 5-6 GHz frequency band.

C_1, C_2, C_3, C_4 are 100 nF decoupling capacitors.

The pad « SW1 » is not used and should be connected to ground.



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DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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ORDERING INFORMATION

Generic type	Package type	Version	Description
CGY2175AUH	Bare Die	C1	3-port C-band Core Chip

RoHS Compliant

Document History : Version 1.1, Last Update 06/2/2013

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