

PRELIMINARY DATASHEET

CGY2179UH/C1

4-bit Ku-Band Core Chip

DESCRIPTION

The CGY2179UH/C1 is a high performance 4-bit Core Chip operating in Ku-band. It includes a 4-bit phase shifter and a LNA. It has a phase shifting range of 360°, and a LSB of 22.5°. It covers the frequency range from 10.7 to 12.75 GHz and can be used in Telecommunication, Radar, Antennas, and Instrumentation applications.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

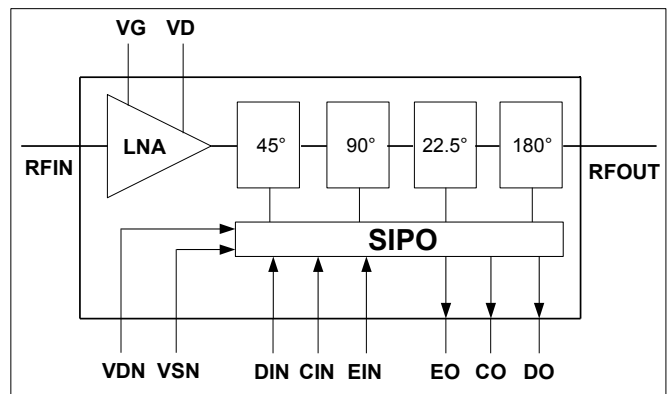
This die is manufactured using OMMIC's 0.18 μm gate length PHEMT Technology ED02AH. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

APPLICATIONS

- ▶ Radar, electrically steerable antennas
- ▶ Telecommunication
- ▶ Instrumentation

FEATURES

- ▶ Operating Range : 10.7 GHz to 12.75 GHz
- ▶ RF Gain ; 12 dB at 11.7 GHz (all states)
- ▶ NF : 1.9 dB at 11.7 GHz (all states)
- ▶ RMS Phase Error : 7° @ 11.7 GHz
- ▶ RMS Amplitude Error : 0.6 dB @ 11.7 GHz
- ▶ Output P1dB : +3 dBm
- ▶ S_{11} : -15 dB at 11.7 GHz (all states)
- ▶ S_{22} : -12 dB at 11.7 GHz (all states)
- ▶ Total Power Consumption : 200 mW
- ▶ Die size : 2.12 x 2.43 x 0.1 mm
- ▶ Delivered as 100% RF tested devices
- ▶ Samples and Demo Board Available



CGY2179UH/C1 Block diagram



LIMITING VALUES

$T_{amb} = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DN}	Positive supply voltage		-1	+6	V
V_{SN}	Negative supply voltage		-6	+1	V
D_{IN} , CLK and LE	Digital data input		-1	+6	V
V_D	Drain voltage		-1	+3	V
V_G	Gate voltage		-0.4	0	V
P_{IN}	Input power			0	dBm
T_j	Junction temperature			+150	°C
T_{stg}	Storage temperature		-55	+150	°C

OPERATING CONDITIONS

$T_{amb} = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DN}	Positive supply voltage		0	+5	V
V_{SN}	Negative supply voltage		-5	0	V
D_{IN} , CLK and LE	Digital data input		0	+5	V
V_D	Drain voltage		0	+2	V
V_G	Gate voltage		-0.4	0	V
P_{IN}	Input power			0	dBm
T_{amb}	Ambient temperature		-40	+85	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient ($T_a = 25\text{ °C}$)	TBD	°C/W

CHARACTERISTICS

RF performances are measured on board at T = 25 °C. Typical RF Performances are given at 11.7 GHz, for the nominal biasing conditions : V_D = +2 V and V_G = -0.3 V.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
<i>DC Supplies</i>						
V _{DN}	Positive supply voltage		4.5	5	5.5	V
I _{DN}	Positive supply current			12		mA
V _{SN}	Negative supply voltage		-5.5	-5	-5.5	V
I _{SN}	Negative supply current			5		mA
V _D	Drain voltage		1.8	2	2.2	V
I _D	Drain current	V _G = -0.3 V		55		mA
<i>RF Performance at 11.7 GHz, V_D = +2V and V_G = -0.3V, unless otherwise specified</i>						
BW	Bandwidth		10.7		12.75	GHz
G	RF Gain		10	12		dB
NF	Noise Figure at reference state			1.9		dB
S ₁₁	Input reflection coefficients (all states)			-15		dB
S ₂₂	Output reflection coefficients (all states)			-12		dB
PH _{Range}	Phase range			+360		°
PH _{error (RMS)}	RMS Phase Error wrt the 16 Phase States			7		°
AMP _{var (RMS)}	RMS Gain Variation wrt the 16 Phase States			0.6		dB
P _{1dB}	Output 1dB compression point			+3		dBm
Rate	Serial data rate			10		Mbps

Note : The RMS value is the root mean square of the error defined as below :

$$x_{RMS} = \sqrt{\frac{1}{N} \sum_{i=1}^N x_i^2} = \sqrt{\bar{x}_i^2 + \sigma_{x_i}^2}$$

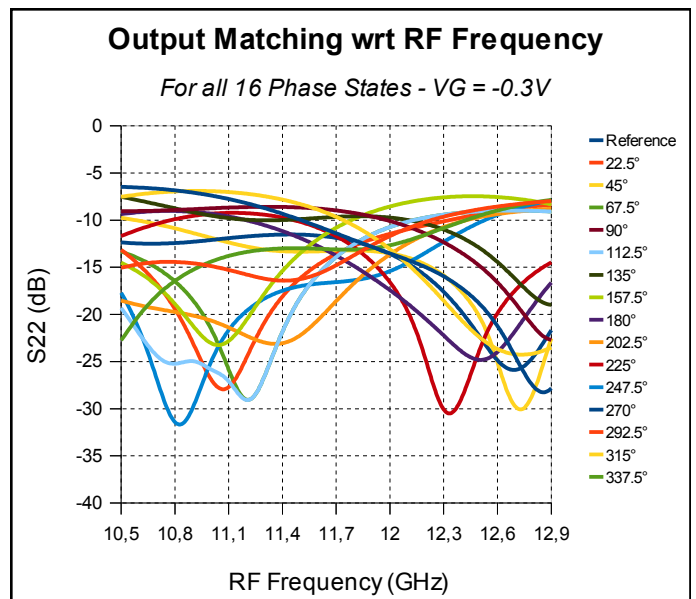
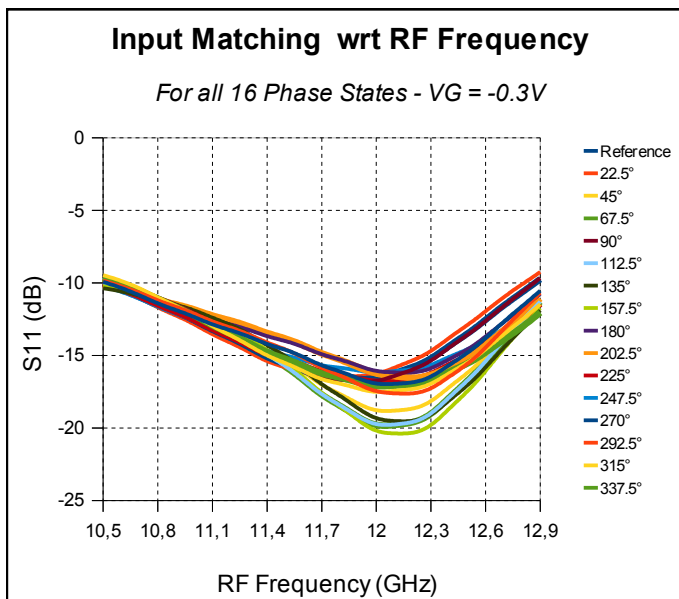
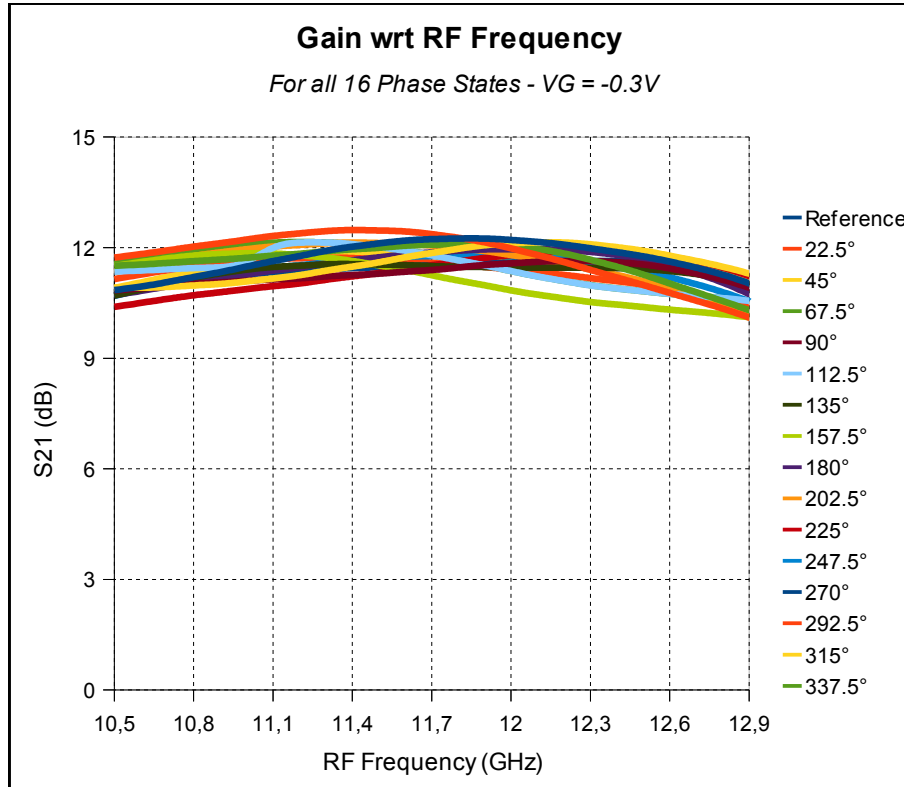
Where x_i is the difference between the measured value and the theoretical value, \bar{x}_i is the mean value of the N x_i, and σ_{x_i} is the standard deviation of x_i.



Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

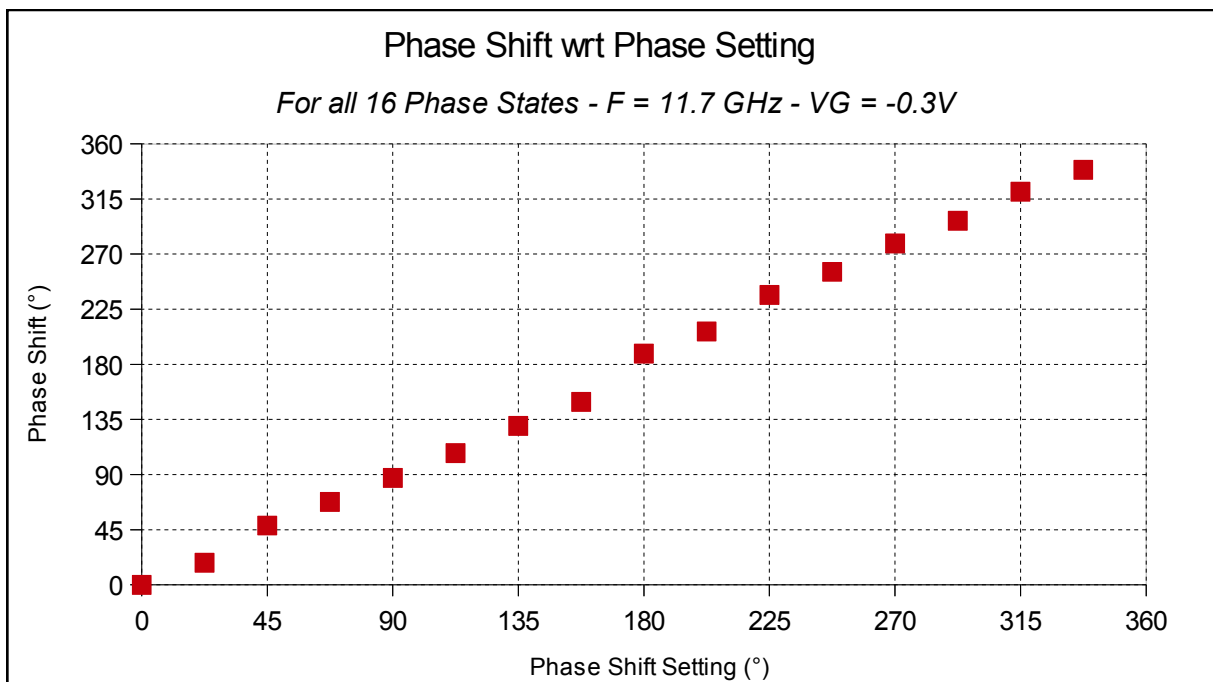
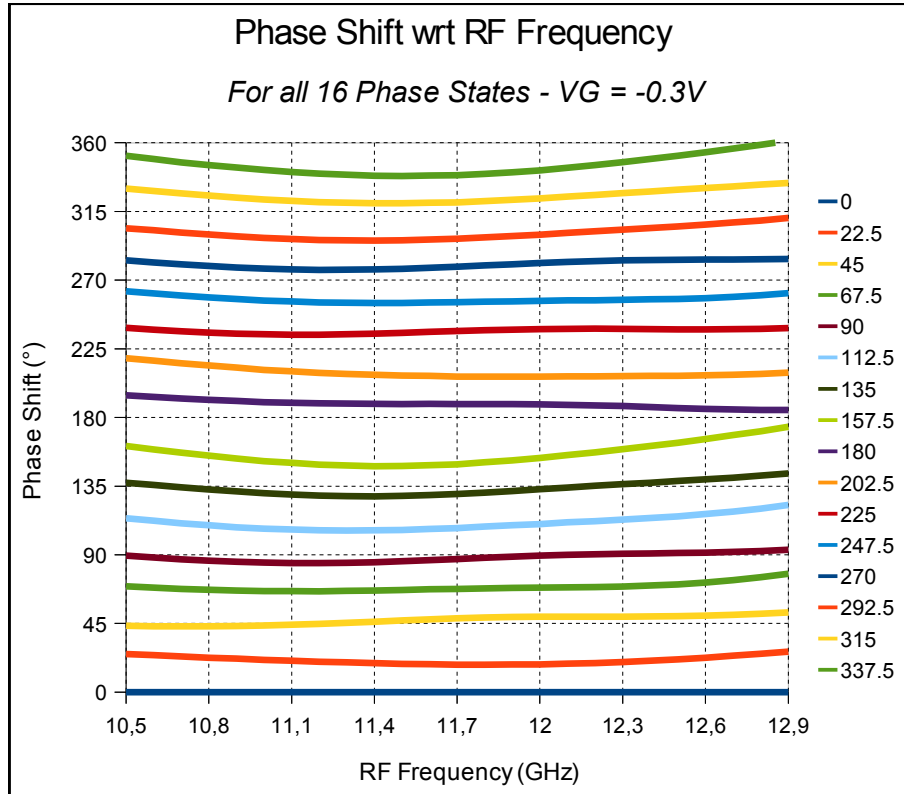
ON BOARD MEASUREMENTS – S PARAMETERS

Measured at nominal power supply voltages and at T = 25 °C.



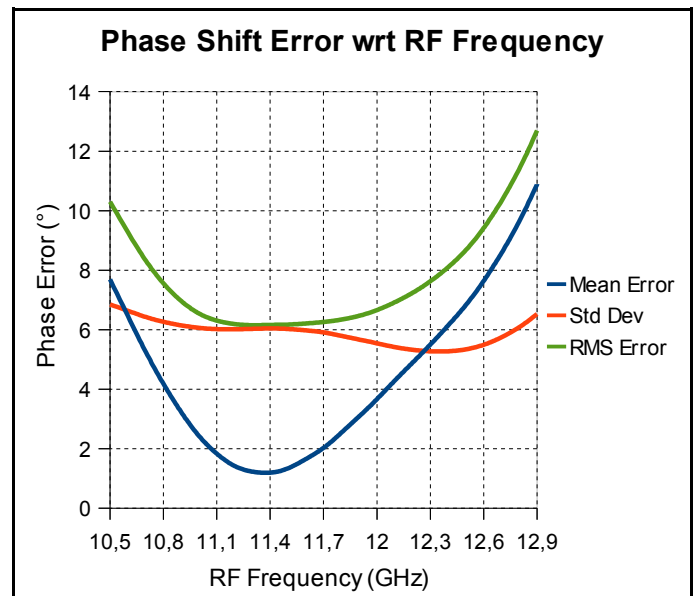
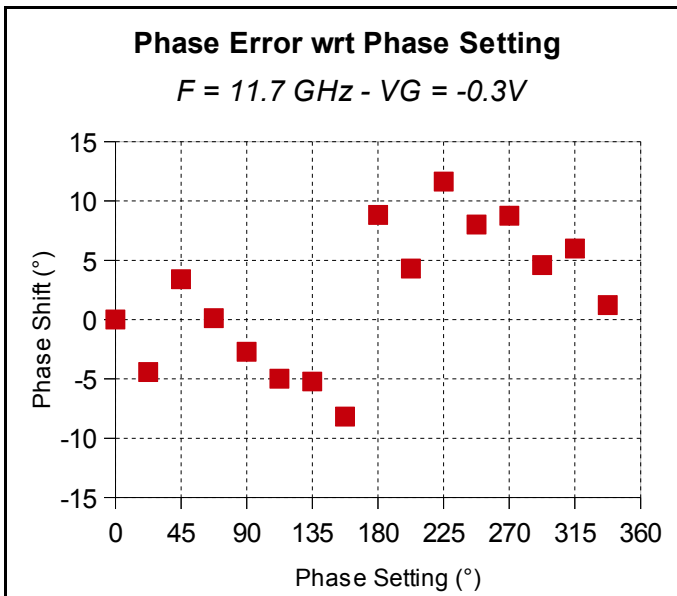
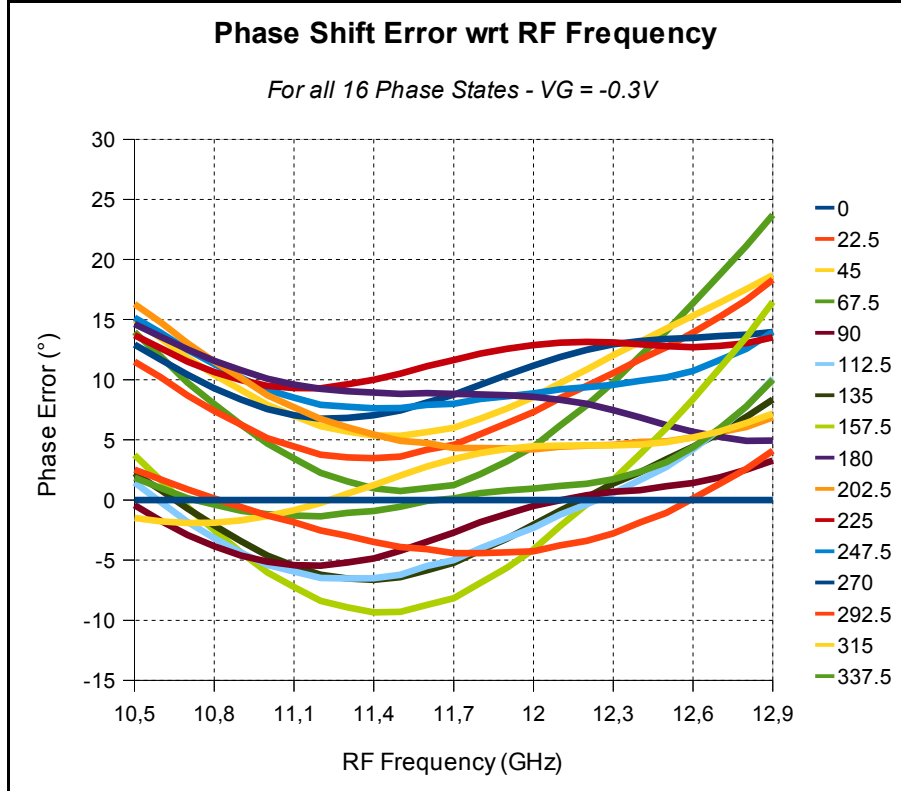
ON BOARD MEASUREMENTS – PHASE SHIFTER RESPONSE

Measured at nominal power supply voltages and at T = 25 °C.



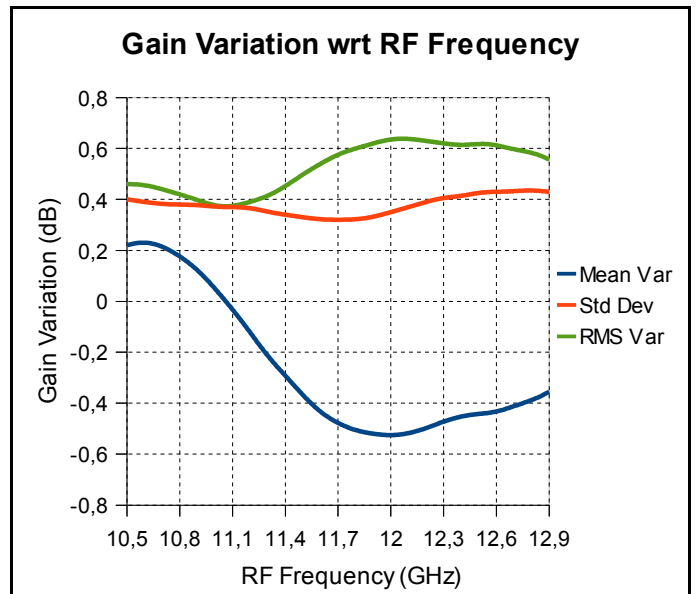
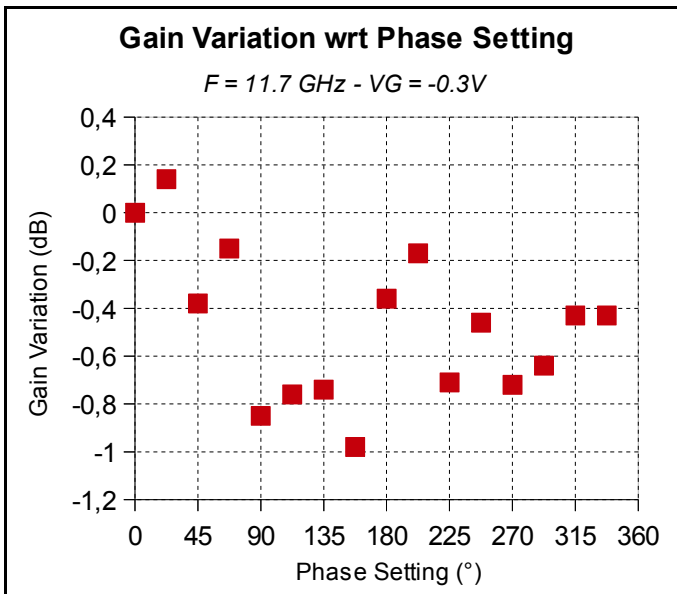
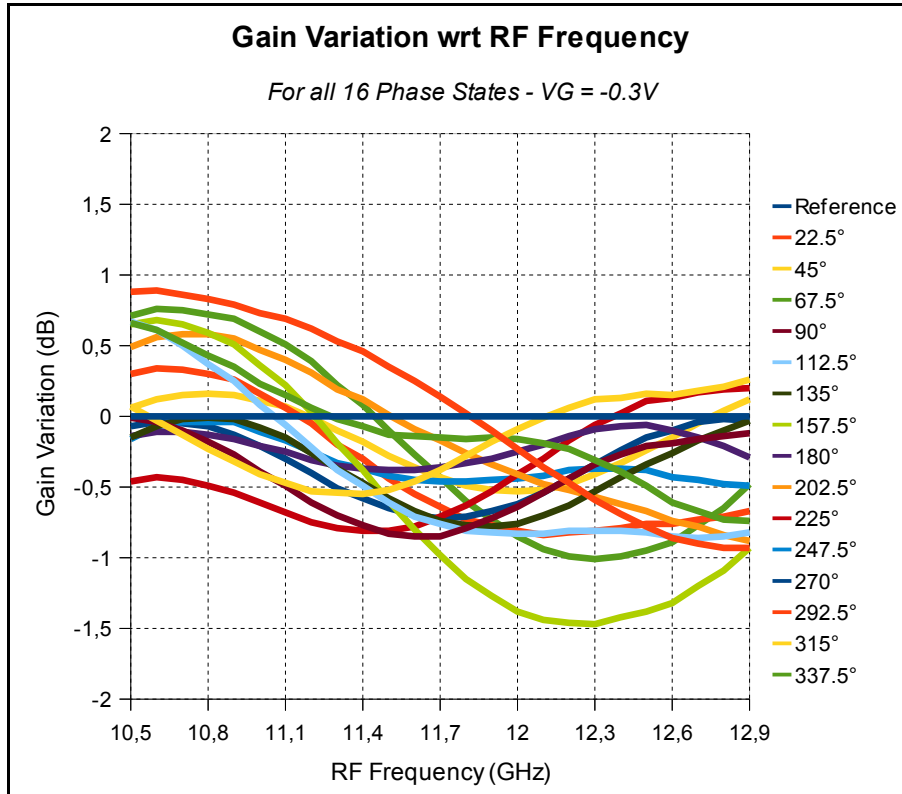
ON BOARD MEASUREMENTS – PHASE SHIFTER ERRORS

Measured at nominal power supply voltages and at T = 25 °C.



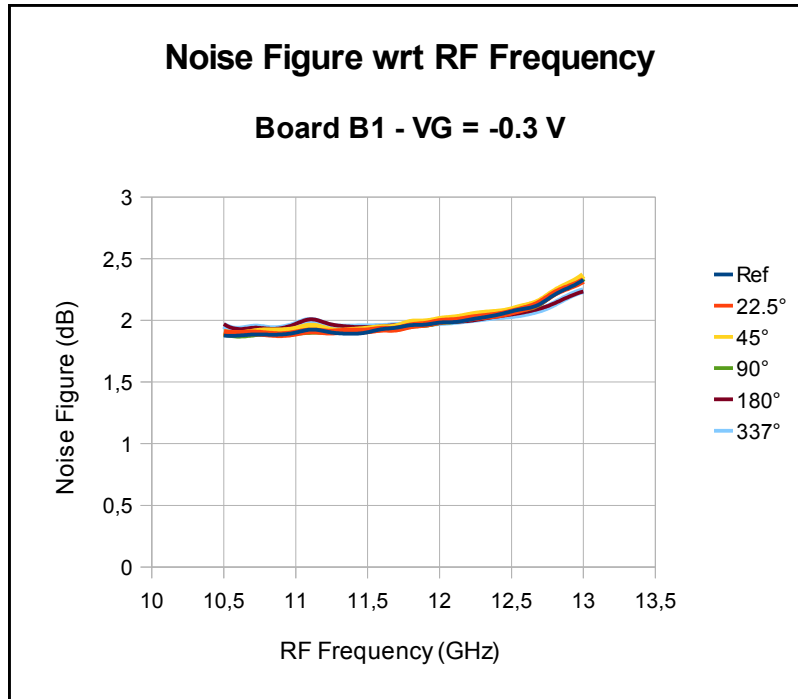
ON BOARD MEASUREMENTS – PHASE SHIFTER ERRORS

Measured at nominal power supply voltages and at T = 25 °C.



ON BOARD MEASUREMENTS – NOISE FIGURE

Measured at nominal power supply voltages and at T = 25 °C.



DATA

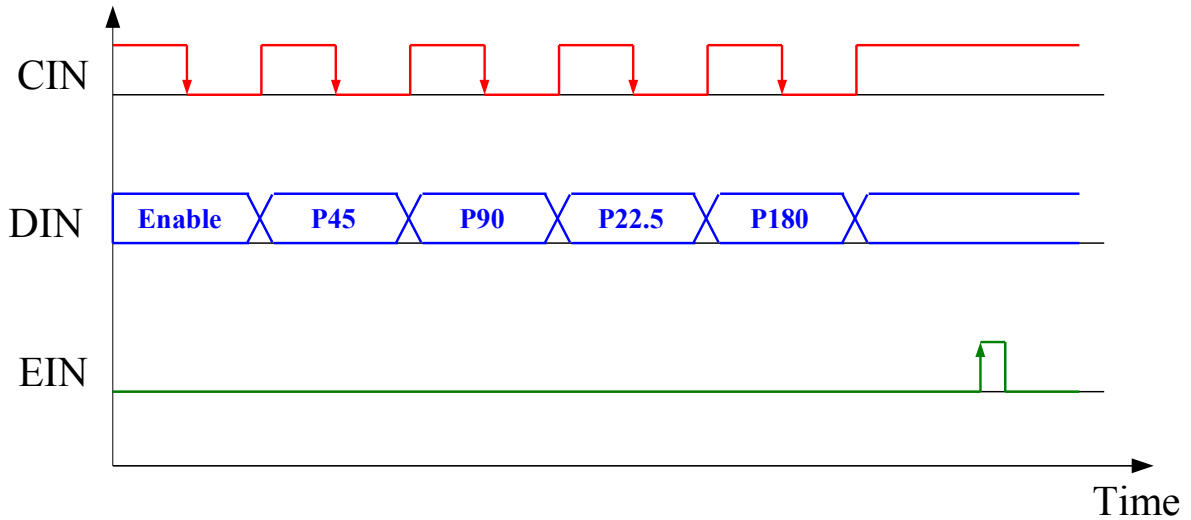
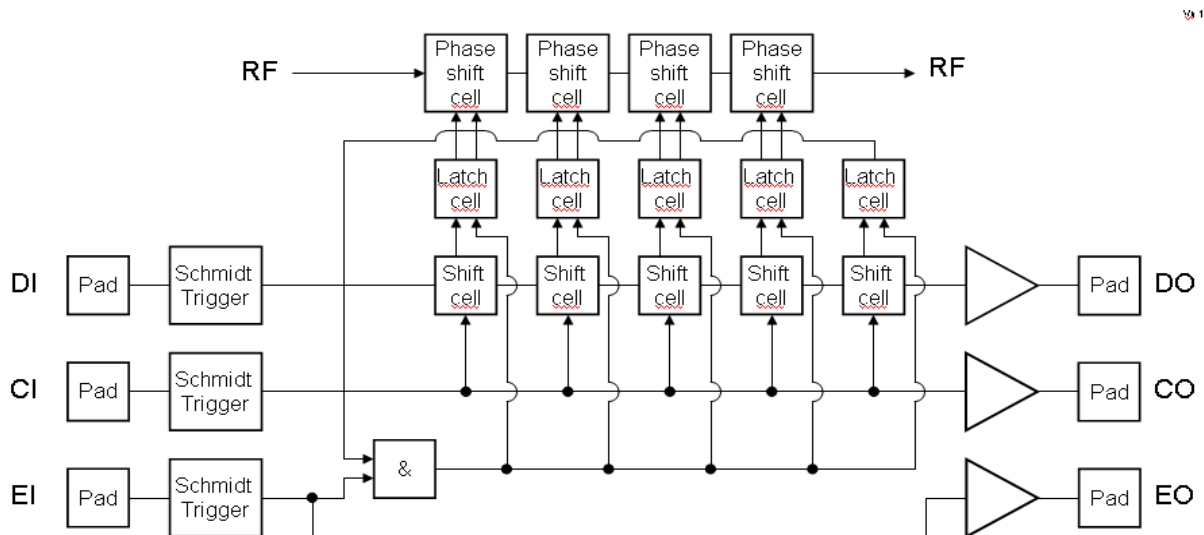
Bit Number	Description	Reference State	Theoretical Value
B0	Enable	Low	-
B1	45° Phase Shifting Cell	Low	45°
B2	90° Phase Shifting Cell	Low	90°
B3	22.5° Phase Shifting Cell	Low	22.5°
B4	180° Phase Shifting Cell	Low	180°

CONTROL VOLTAGE (CMOS STANDARD LOGIC)

State	Vmin	Vmax
Low	0 V	1 V
High	+3 V	V _{DN}

TIMING DIAGRAM

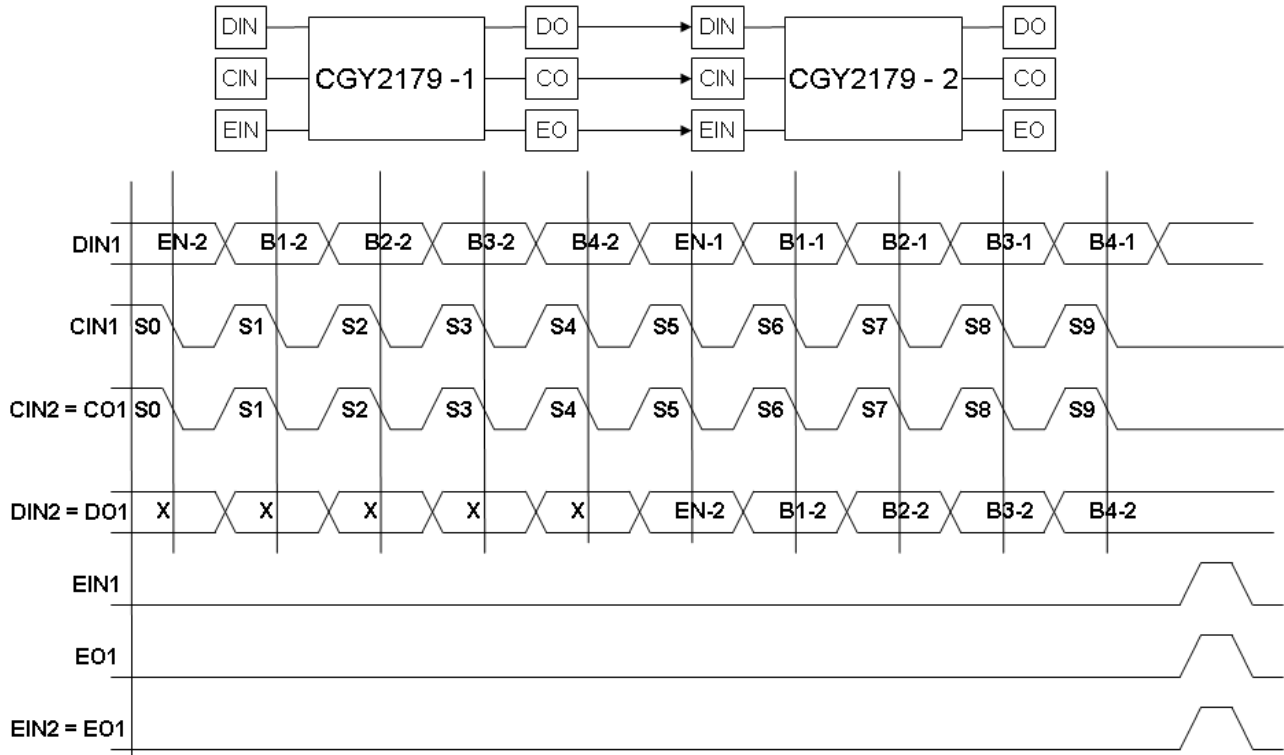
- DIN is sampled at the falling edge of CIN.
- Falling edge of EIN must occur when all the 5 bits are loaded and on high level of CIN.
- DIN is transferred and Phase Shifter positions changed on high level of EIN.


INTERNAL CONTROL BLOCK DIAGRAM


CASCADED CGY2179UH/C1 CONTROL

2 or more CGY2179UH/C1 can be cascaded and controlled by a unique serial interface.

The enable/disable bit and associated internal hardware allow the user to chose the devices which are not subject to reprogramming in the device chain.

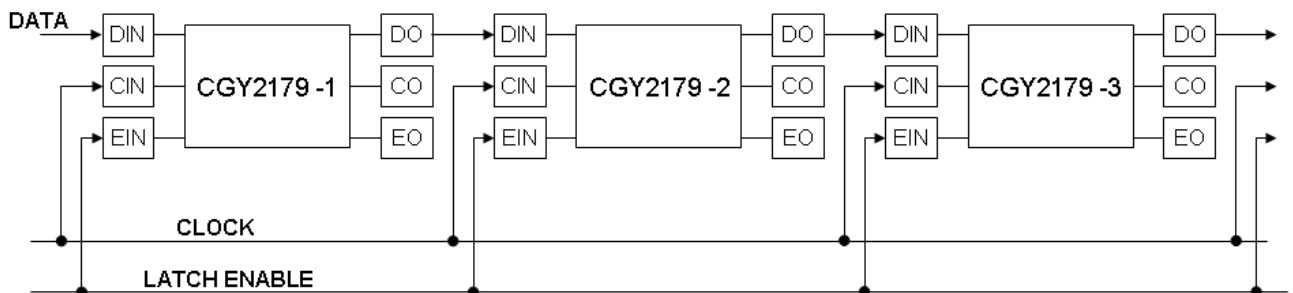


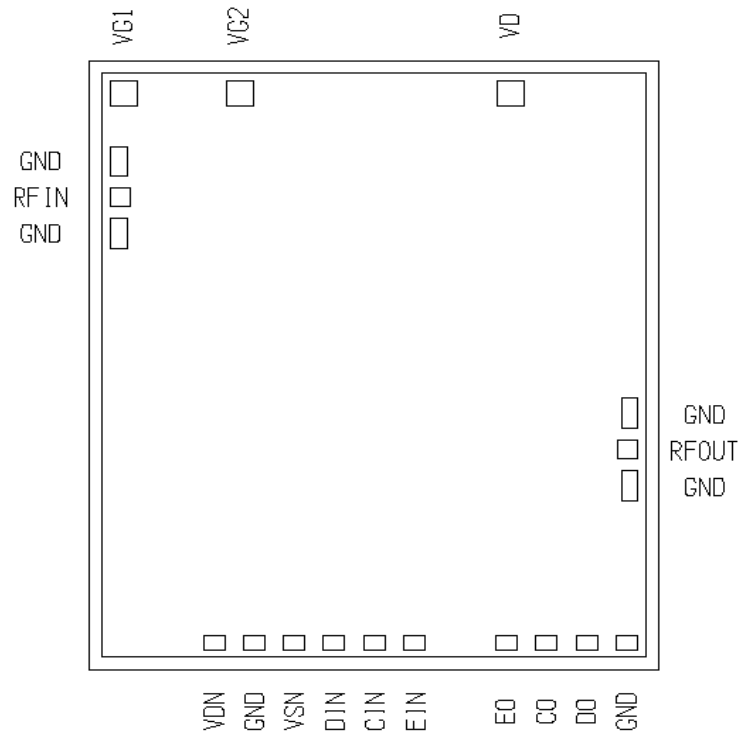
DAISY CHAIN CONFIGURATION

An alternate way of designing a multiple CGY2179UH/C1 system using a single serial interface is to use the daisy chain mechanism.

Output data pin DO of device number N is connected to Input data pin DIN of device number N+1, Clock and LATCH ENABLE pin are driven in parallel

The enable/disable bit and associated internal hardware allow the user to chose the devices which are not subject to reprogramming in the device chain.



PAD CONFIGURATION


SYMBOL	PAD	DESCRIPTION
GND	GND	Ground
RFIN	RFIN	RF Input
VDN	VDN	Positive Supply Voltage
VSN	VSN	Negative Supply Voltage
DIN	DIN	Data Input
CIN	CIN	Clock Input
EIN	EIN	Enable Input
EO	EO	Data Output
CO	CO	Clock Output
DO	DO	Enable Output
RFOUT	RFOUT	RF Output
VD	VD	Drain Voltage
VG1	VG1	Gate Voltage first stage LNA
VG2	VG2	Gate Voltage second stage LNA

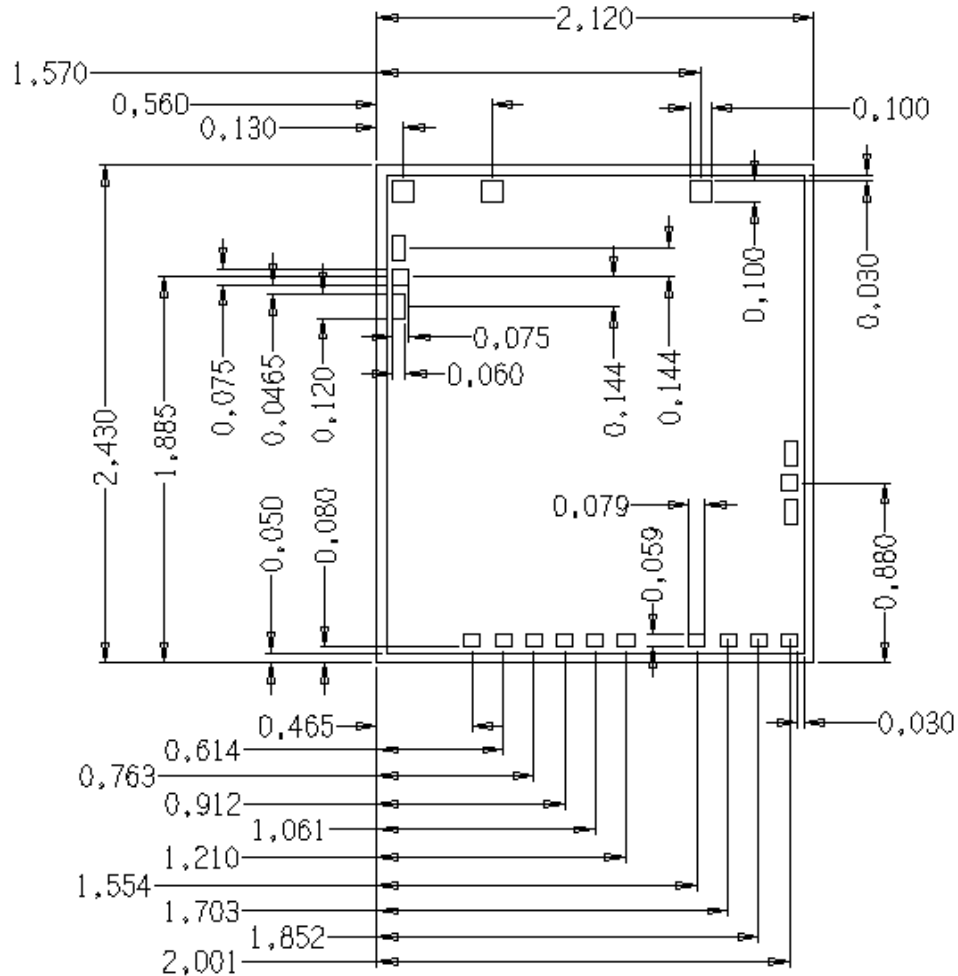
Note :

It is essential in order to ensure good performance and stability that the backside of the die is suitably connected to the ground.



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PAD COORDINATES



Notes 1 : RFIN and RFOUT pads are suitable to accommodate GSG 150 μm RF probes

- Central pad (Signal) is 75 x 75 μm
- Lateral pads (GND) are 120 x 60 μm
- Distance from central pad to ground pads are 46.5 μm
- Distance from pad to dicing streets are 30 μm

Notes 2 : Control pad

- North pads are 100 x 100 μm
- South pads are 79 x 49 μm
- Distance from pad to dicing streets are 30 μm

Notes 3 : Dicing reduce the device by approximately 32 μm

ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2179UH	Die	C1	-	4-bit Ku-band Core Chip



DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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