

PRELIMINARY DATASHEET

CGY2351UH/C1 26.5 – 30.5 Ghz 2 ports Corechip

DESCRIPTION

The CGY2351UH/C1 is a high performance GaAs MMIC Core Chip operating in Ka-band. It follows the T/R architecture, is passive, and exhibits only 2 RF ports. It includes a 6 bit Phase shifter and a 5 bits attenuator; it has a phase shift range of 360° with a 5.62° step and attenuation range of 22 dB with 0.7 dB step. It operate from 26.5 to 30.5 GHz.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interface with this device.

This die is manufactured using OMMIC's 0.18 μm gate length ED02AH PHEMT Technology. The MMIC uses gold bonding pads and backside metallization. It is fully protected by a Silicon Nitride passivation layer to obtain the highest level of reliability. This technology has been evaluated for Space applications by the European Space Agency (ESA) and is on the European Preferred Parts List of ESA.

APPLICATIONS

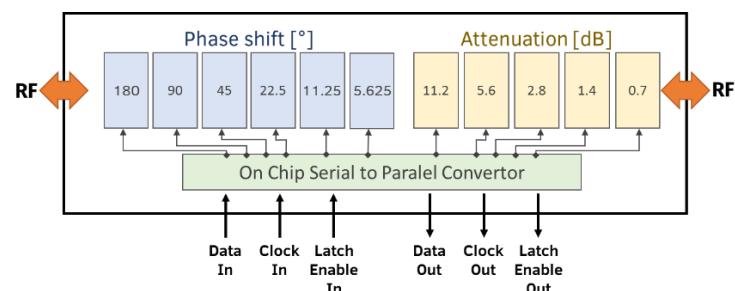
- Radar
- Telecommunication
- Instrumentation

Revision : 25/08/2016

Website : www.ommic.com

FEATURES

- ▶ Operating Range: 26.5 to 30.5 GHz
- ▶ Phase Shifter 6 bits: 360° max with 5.625° step
- ▶ Attenuation 5 bits; 22dB max 0.7 dB step
- ▶ RMS Phase Error : 4 ° all states
- ▶ RMS Amplitude Error : 0.5 dB all states
- ▶ Input matching IRL: 14 dB
- ▶ Output matching ORL: 13 dB
- ▶ Supply voltage +5 & -5 V
- ▶ Total current consumption 17 mA
- ▶ Chip size = 4.8 x 1.6 mm
- ▶ Device Availability : Available
 - Tested, Inspected Known Good Die (KGD)
 - Space and MIL-STD MMIC's



CGY2351UH/C1 Block diagram

OMMIC

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LIMITING VALUES

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V _{DN}	Control I/O Pins voltage		0	5.5	V
V _{SN}	Control I/O Pins voltage		-5.5	0	V
I _{D total}	Total Drain current			100	mA
T _{stg}	Storage temperature		-55	+150	° C
T _j	Junction temperature			+150	° C
T _{amb}	Ambient temperature		-40	+85	° C

Operating this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
R _{th(j-a)}	Thermal resistance from junction to ambient (T _a = 25 °C)	TBD	° C/W

DC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
V _{DN}	Positive supply voltage		0	5	5.5	V
I _{DN}	Positive supply current		3	5	8	mA
V _{SN}	Negative Supply voltage		-5.5	-5	-4.5	V
I _{SN}	Negative supply current		10	12	15	mA

RF CHARACTERISTICS
 $T_{amb} = 25\text{ °C}$, $V_{DN} = +5.0\text{ V}$, $V_{SN} = -5.0\text{ V}$

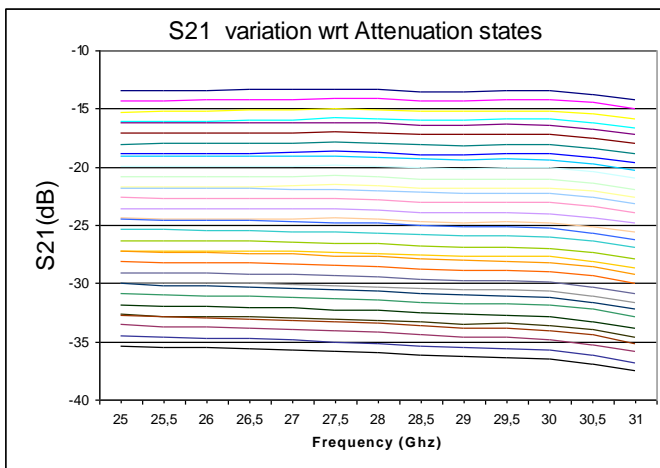
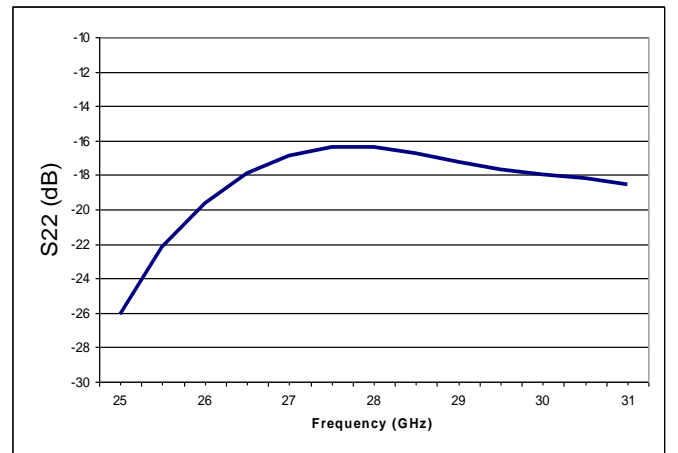
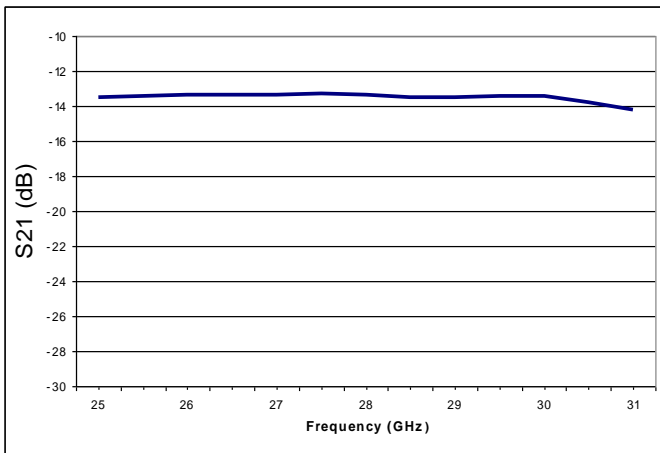
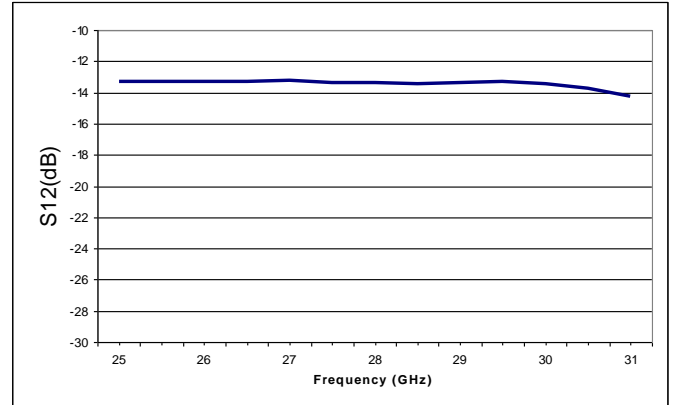
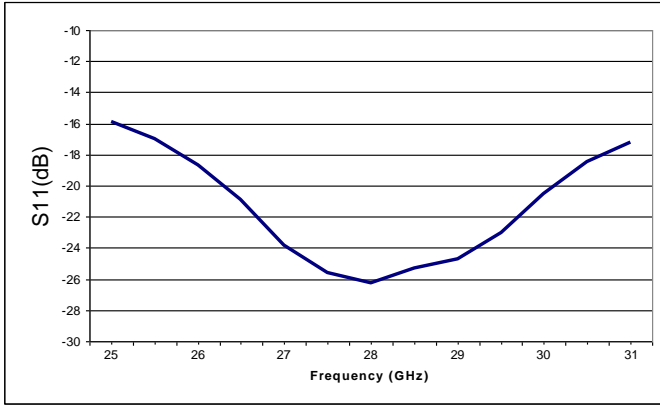
 Specifications using 50 Ω RF pads, unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Frequency	Frequency Bandwidth		26.5		30,5	GHz
S21	Insertion Loss		-17	-15	-13	dB
S11	Input return loss			-14	-12	dB
S22	Output return loss			-14	-12	dB
PSrange	Phase Shift range			360		°
PSstep	Phase Shift step			5.625		°
PSrmserr	Phase Shift RMS Error	27.5 Ghz à 30 GHz	2	4	6	°
ATTrange	Attenuator Range			21.7		dB
ATTrmserr	Attenuator RMS Error	27.5 Ghz à 30 GHz		0.5	1.2	dB
P1dB	Input P1 dB	VL=-2 V, all attenuator off, all phase shifter off	20.5			dBm

ON WAFER MEASUREMENTS S-PARAMETERS

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{DN} = +5.0\text{ V}$, $V_{SN} = -5.0\text{ V}$

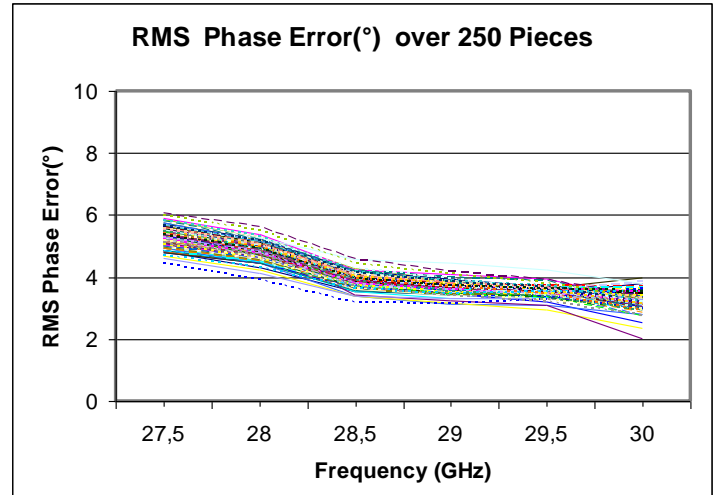
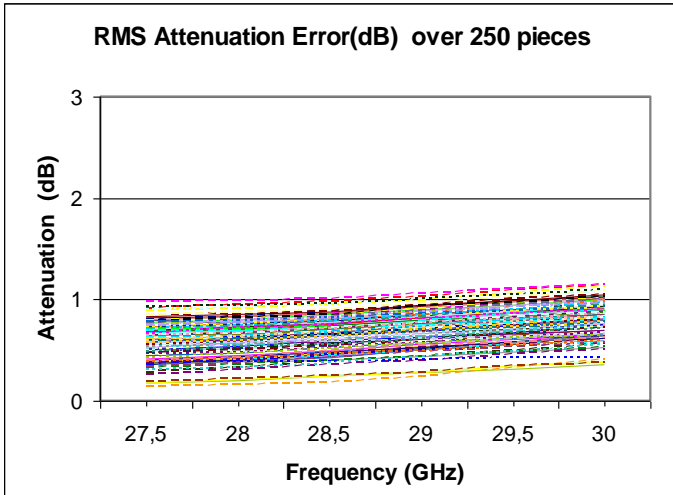
Corrected with Input and Output Inductance of 0.3 nH to take into account the bonding inductance.



ON WAFER MEASUREMENTS RMS ERRORS

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{DN} = +5.0\text{ V}$, $V_{SN} = -5.0\text{ V}$

Corrected with Input and Output Inductance of 0.3 nH to take into account the bonding inductance



SERIAL TO PARALLEL INTERFACE (SIPO) :

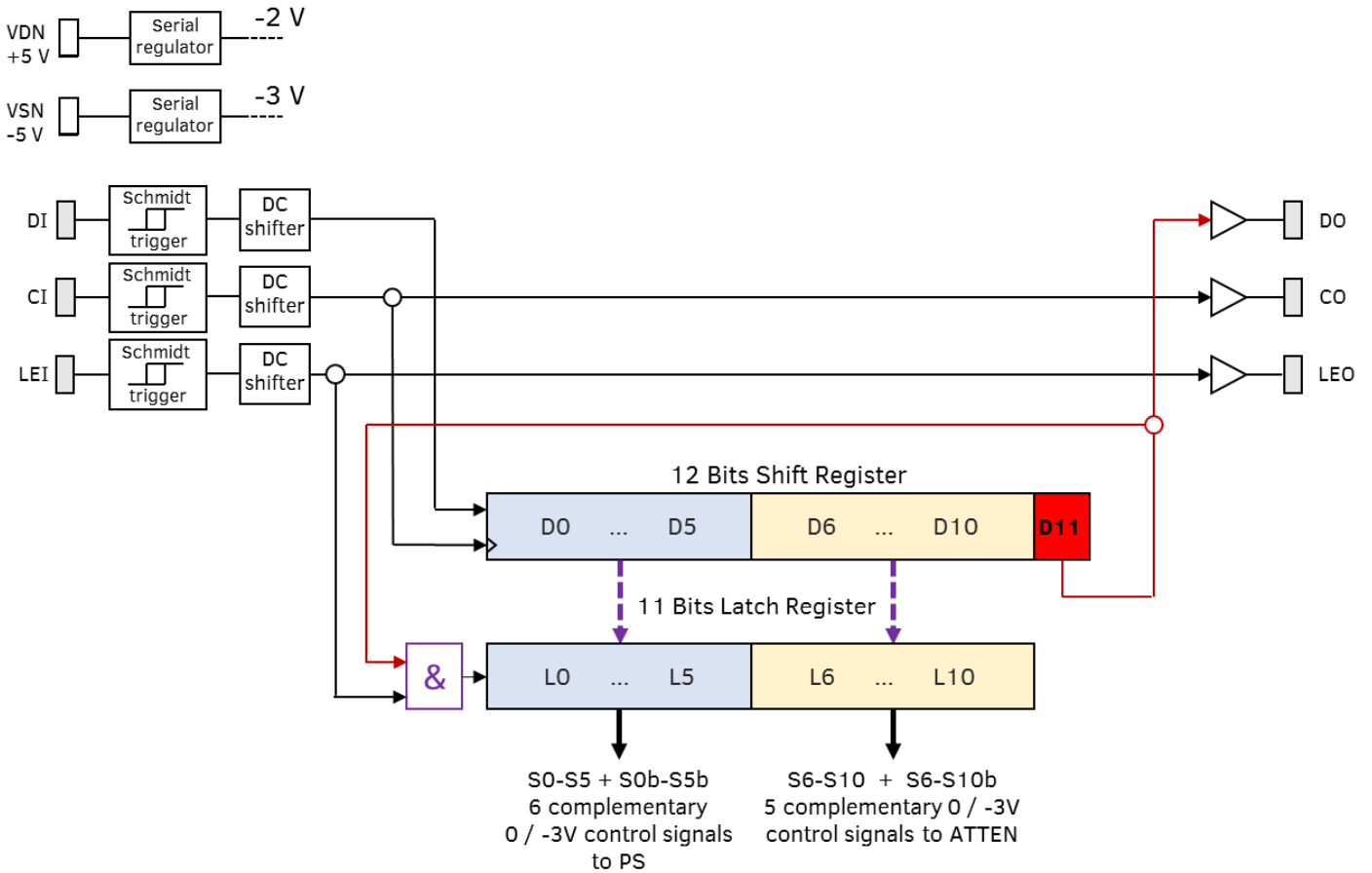


Figure 1: functional block diagram

Name	Definition	Value	Comment
DI	Data In	0/+5 V	
CI	Clock In	0/+5 V	Active on rising edge
LEI	Latch Enable In	0/+5 V	Active high 5 V
DO	Data Out	0/+5 V	Copy of D11 (first bit loaded)
CO	Clock Out	0/+5 V	Copy of CI, delayed by buffers (≈2 to 5 ns)
LEO	Latch Enable Out	0/+5 V	Copy of LEI, delayed by buffers (≈2 to 5 ns)
VDN	Positive Power Supply	+5 V ±5 %	Current 2 to 4 mA
VSN	Negative Power Supply	-5 V ±5 %	Current 10 to 15 mA
S0-S5 S0b-S5b	Phase-Shifter Control	0/-3 V -3/0 V	6 complimentary signals for phase-shifter state
S6-S10 S6b-S10b	Attenuator Control	0/-3 V -3/0 V	5 complimentary signals for attenuator state

TIMING DIAGRAM (SIPO)

Data In is sampled at the rising edge of the *Clock In* signal.

Rising edge of LEI (Latch Enable In) must occur after all 12 bits are loaded.

Data In is transferred to the operating register (and Attenuator/Phase Shifter settings are changed) on the rising edge of *Latch Enable In* hardware line if the D11 bit (the first one to be sent) is equal to 1.

The Clock defines the speed of changing Attenuator/Phase Shift setting, the setting could be changed in 600 ns (if 20 MHz Clock) or 54 ns (if 240 MHz Clock).

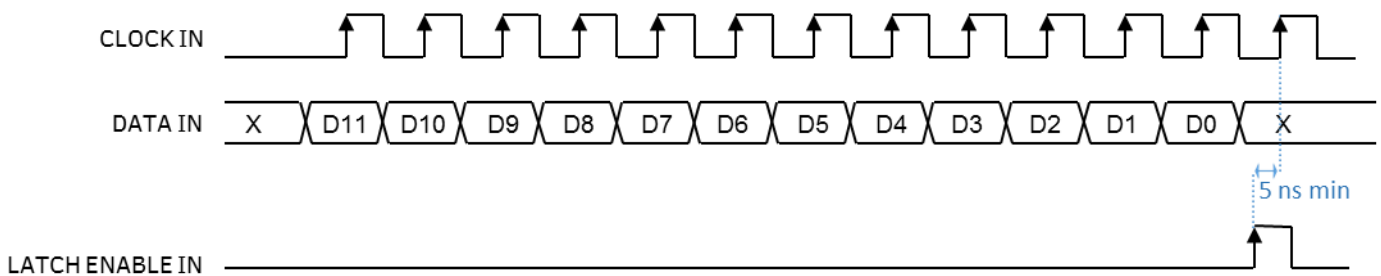


Figure 2: Control Interface timing diagram

In order to simplify the control of multiple devices using the same bit stream and to improve the resistance of the control to glitches, an additional control bit has been implemented in the control bit stream.

Bit D11 is a change enabled bit; the state of the CGY2351UH/C1 device can be changed only when D11=1 and the Latch Enable (In) hardware line is toggled (c.f. figure 1).

Bit number	Use	Value	Unit
D11	Enable change on Latch Enable pulse	0 / 1	–
D10	Attenuation state control	-0.7	dB
D9	Attenuation state control	-1.4	dB
D8	Attenuation state control	-2.8	dB
D7	Attenuation state control	-5.6	dB
D6	Attenuation state control	-11.2	dB
D5	Phase state control	5.625	°
D4	Phase state control	11.3	°
D3	Phase state control	22.5	°
D2	Phase state control	45	°
D1	Phase state control	90	°
D0	Phase state control	180	°

Table 1: Bit allocation

Setup and hold times should be greater than **5 ns** :

- For DI and LEI with respect to CI rising edge
- For LEI with respect to CI falling edge

In order to reduce wiring volume and weight in user application, the user could use multiple devices in a cascaded architecture as shown in the figure below.

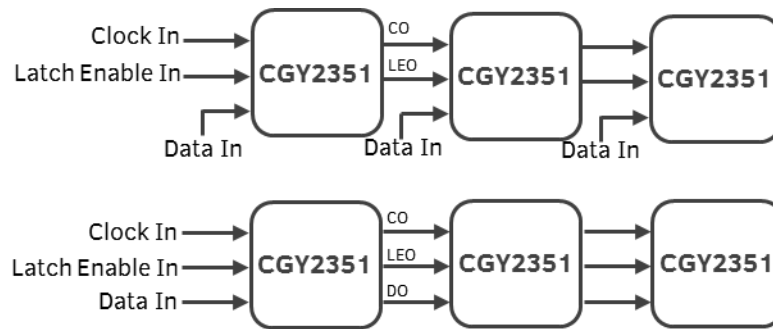


Figure 3: Examples of Cascaded Corechips

S-PARAMETERS

Corrected data, at reference state

FREQ (GHz)	S11M	S11A°	S21M	S21A°	S12M	S12A°	S22M	S22A°
1,000	0,684	-44,6	0,001	147,2	0,001	161,1	0,837	-52,2
2,000	0,282	-39,9	0,005	102,9	0,005	101,3	0,515	-104,0
3,000	0,368	-8,4	0,011	54,0	0,011	54,2	0,283	170,4
4,000	0,512	-18,1	0,017	11,1	0,017	10,9	0,296	112,4
5,000	0,585	-35,3	0,024	-28,7	0,024	-27,9	0,425	68,1
6,000	0,598	-54,5	0,032	-65,6	0,032	-65,6	0,544	39,8
7,000	0,562	-75,3	0,041	101,8	0,042	102,2	0,633	17,5
8,000	0,477	-98,4	0,053	138,6	0,053	139,3	0,691	-2,2
9,000	0,348	125,3	0,067	175,7	0,067	176,7	0,720	-20,2
10,000	0,187	162,2	0,084	144,6	0,083	144,1	0,720	-37,6
11,000	0,077	96,2	0,102	105,2	0,102	104,1	0,693	-54,4
12,000	0,187	10,5	0,122	61,4	0,121	62,6	0,644	-70,6
13,000	0,280	-26,3	0,140	20,2	0,139	20,4	0,576	-86,2

14,000	0,302	-55,0	0,157	-22,8	0,156	-22,1	0,496	-	101,2	
15,000	0,259	-77,7	0,171	-65,5	0,170	-65,2	0,412	-	116,3	
16,000	0,186	-89,8	0,184	-	109,0	0,183	108,6	0,327	-	131,3
16,500	0,153	-88,9	0,188	-	129,9	0,187	129,7	0,284	-	139,4
17,000	0,133	-82,9	0,193	-	151,1	0,192	150,5	0,240	-	147,8
17,500	0,129	-75,4	0,195	-	172,0	0,195	171,4	0,195	-	157,0
18,000	0,136	-71,1	0,199	-	167,4	0,199	167,3	0,149	-	166,5
18,500	0,143	-70,6	0,202	-	146,7	0,202	146,4	0,103	-	176,6
19,000	0,148	-73,0	0,206	-	124,7	0,207	125,0	0,058	-	172,8
19,500	0,146	-76,0	0,211	-	103,3	0,212	104,0	0,016	-	159,7
20,000	0,140	-78,0	0,214	-	82,1	0,215	82,3	0,020	-	-30,7
20,500	0,131	-77,7	0,216	-	60,9	0,217	61,0	0,049	-	-42,2
21,000	0,127	-74,8	0,217	-	38,9	0,219	39,2	0,069	-	-54,2
21,500	0,130	-71,0	0,219	-	17,5	0,220	17,7	0,079	-	-66,1
22,000	0,141	-69,1	0,219	-	-4,2	0,218	-4,1	0,079	-	-77,0
22,500	0,155	-71,1	0,217	-	-25,9	0,220	-25,3	0,070	-	-87,0
23,000	0,169	-76,0	0,217	-	-47,5	0,220	-46,9	0,054	-	-95,0
23,500	0,178	-83,3	0,217	-	-68,9	0,218	-68,9	0,033	-	-94,7
24,000	0,180	-92,1	0,215	-	-90,0	0,219	-90,0	0,016	-	-52,3
24,500	0,174	-	0,213	-	111,6	0,216	111,8	0,031	-	1,6
25,000	0,161	-	0,213	-	132,8	0,216	133,2	0,056	-	7,6
25,500	0,142	-	0,215	-	154,4	0,217	154,5	0,083	-	2,7
26,000	0,118	-	0,215	-	176,5	0,217	176,2	0,110	-	-5,5
26,500	0,093	-	0,216	-	161,3	0,218	160,9	0,131	-	-15,2
27,000	0,070	-	0,216	-	138,6	0,219	137,9	0,146	-	-24,8
27,500	0,054	-	0,218	-	115,6	0,215	115,3	0,156	-	-34,4
28,000	0,050	-	0,217	-	92,5	0,215	92,0	0,157	-	-43,5
28,500	0,052	-96,0	0,213	-	68,6	0,214	69,4	0,152	-	-51,5
29,000	0,058	-88,9	0,212	-	45,1	0,215	45,5	0,143	-	-57,4
29,500	0,070	-83,2	0,214	-	21,2	0,216	20,9	0,132	-	-60,5
30,000	0,094	-85,6	0,213	-	-4,2	0,213	-4,6	0,126	-	-61,9
30,500	0,120	-99,0	0,206	-	-30,3	0,206	-30,6	0,122	-	-64,2

31,000	0,138	-	115,7	0,195	-56,4	0,194	-56,0	0,115	-66,9
31,500	0,152	-	134,0	0,186	-81,3	0,185	-80,9	0,108	-68,2
32,000	0,160	-	153,3	0,176	-	105,7	105,4	0,101	-68,9
32,500	0,165	-	172,7	0,170	-	130,4	132,0	0,096	-68,5
33,000	0,166	-	167,3	0,162	-	155,7	157,0	0,090	-67,6
33,500	0,164	-	148,9	0,156	178,4	0,156	176,3	0,085	-67,1
34,000	0,160	-	132,1	0,149	151,3	0,150	151,4	0,079	-66,1
34,500	0,154	-	118,0	0,144	123,1	0,142	122,6	0,071	-63,2
35,000	0,150	-	106,5	0,137	93,4	0,136	93,6	0,063	-57,1
35,500	0,144	-	97,9	0,128	62,0	0,126	61,7	0,057	-43,5
36,000	0,141	-	91,8	0,117	29,1	0,116	27,6	0,063	-23,6
36,500	0,139	-	87,9	0,103	-6,2	0,101	-7,1	0,087	-10,4
37,000	0,139	-	87,9	0,085	-43,6	0,085	-44,3	0,127	-9,6
37,500	0,152	-	92,2	0,065	-82,2	0,065	-81,7	0,172	-17,4
38,000	0,192	-	93,0	0,045	-	120,0	120,2	0,215	-28,7
38,500	0,244	-	84,8	0,027	-	154,8	156,2	0,251	-42,4
39,000	0,283	-	72,1	0,015	176,7	0,014	175,0	0,271	-56,9
39,500	0,297	-	58,7	0,007	152,5	0,007	154,1	0,275	-71,0
40,000	0,284	-	46,5	0,003	147,6	0,003	147,6	0,265	-83,6

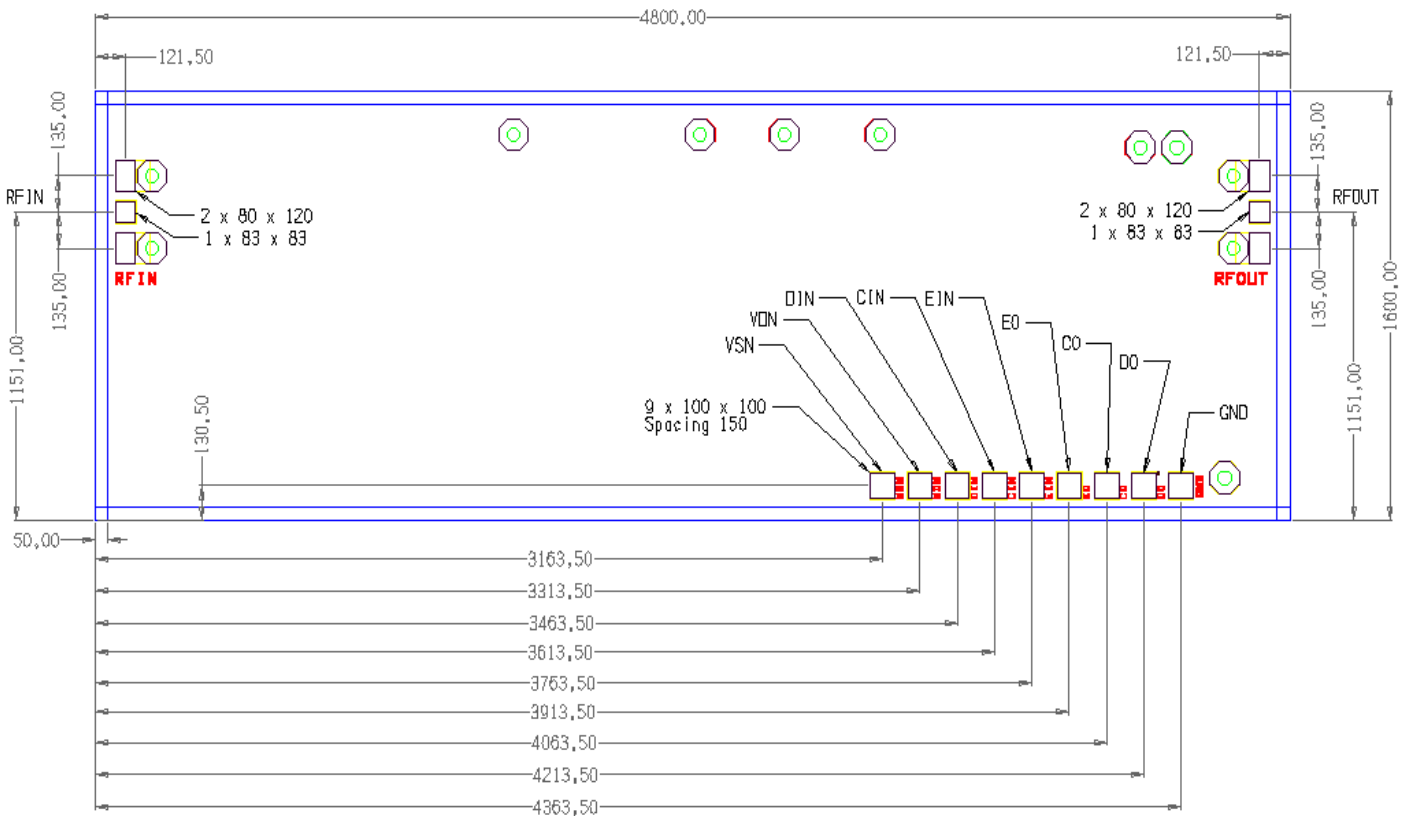
PINOUT

Symbol	Pad	Description
RF1	RFOUT	RF port 1 (device is bidirectional)
RF2	RF IN	RF port 2 (device is bidirectional)
VDN	VDD	Positive supply Pad
VSN	VSN	Negative supply pad
DIN, CIN,EIN	DIN, CIN,EIN	SIPO Input (Data, Clock, Latch Enable)
DO,CO,EO	DO,CO,EO	SIPO Output (Data, Clock, Latch Enable)
GND	BACKSIDE	Ground

MECHANICAL INFORMATION

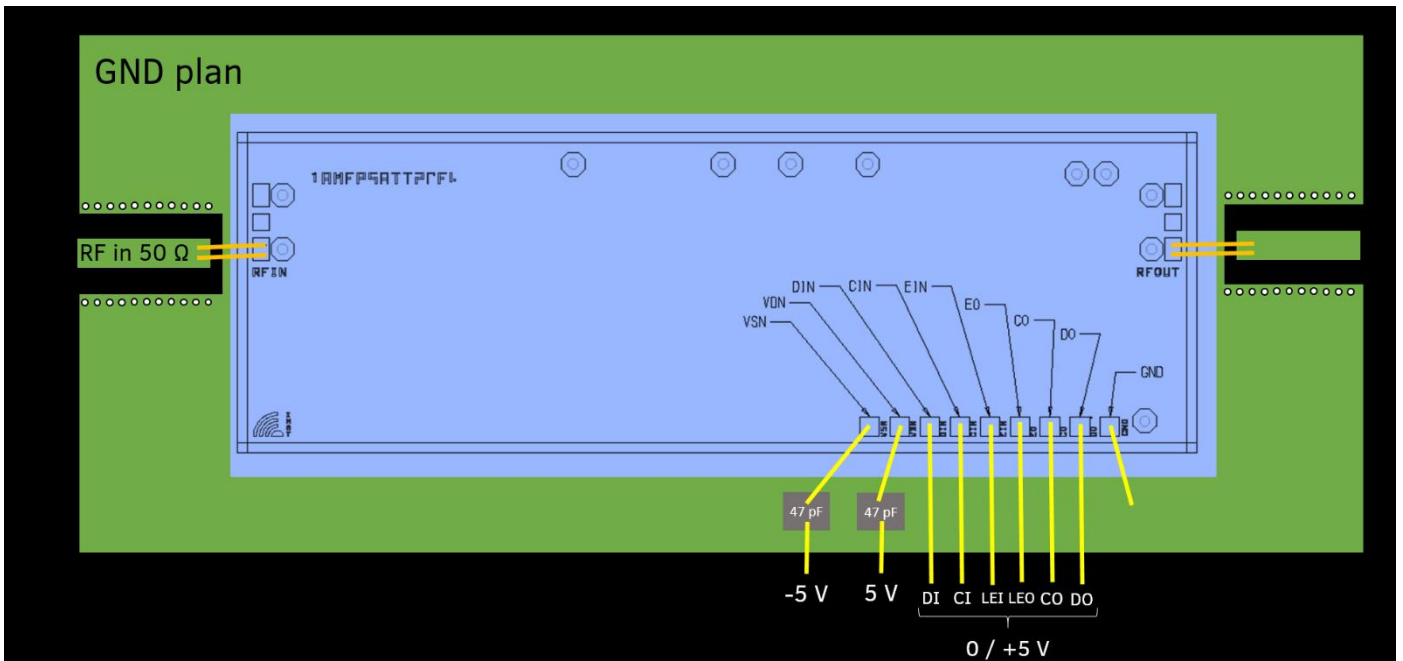
Chip size : 4.8 x 1.6 mm
 RF Pads: see details below
 DC Pads : 100 x 100 µm
 Chip thickness : 100µm

All sizes indicated below are in microns



RF Bondings: 2 bondings with 25 μm in diameter and with a maximum length of 200 μm (150 μm recommended)

DC Bonding: 1 bonding with 25 μm in diameter can be used



ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2351	UH	C1	-	On-Wafer measured Die
CGY2351UH/C1/EK				Evaluation Board



Caution: This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are only stress ratings and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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