

PRELIMINARY DATASHEET

CGY2125AUH/C1

Low Noise 13-15 GHz Amplifier

DESCRIPTION

The CGY2125AUH/C1 is a high performance GaAs Low Noise Amplifier MMIC designed to operate in the Ku band.

The CGY2125AUH/C1 has a low noise figure of 1.7 dB with 25 dB of gain for a power consumption of only 65mW. On chip matching provides 11 dB of Input Return Loss and 20dB Output Return Loss at 14 GHz. It can be used in Radar, Telecommunication and Instrumentation applications.

The die is manufactured using OMMIC's 0.13 μm gate length PHEMT Technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

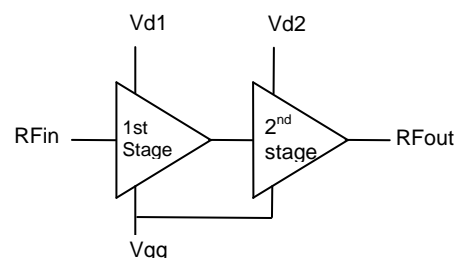
This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

APPLICATIONS

- Radar
- Telecommunications
- Instrumentation

FEATURES

- ▶ Operating Range : 13 GHz to 15 GHz
- ▶ Noise 1.5 dB at 14 GHz
- ▶ Gain : 25 dB at 14 GHz
- ▶ Output $P_{1\text{dB}}$: 8 dBm
- ▶ Input Return Loss : > 11 dB at 14 GHz
- ▶ Output Return Loss : > 20 dB at 14 GHz
- ▶ Power Supply : 20 mA at 3.3 V
- ▶ Single Supply device when using $V_{\text{gg}} = 0\text{ V}$
- ▶ Chip size = 2.2 mm x 1.1 mm
- ▶ Device Availability :
 - Tested, Inspected Known Good Die (KGD)
 - Demonstration Boards
 - Space and MIL-STD MMICs



CGY2125AUH/C1 block diagram



MAXIMUM VALUES

$T_{amb} = + 25 \text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{gg}	Gate voltage	V_{DD} Open circuit	- 4	1	V
V_{d1}, V_{d2}	Drain voltage	V_{DD} Open circuit	-4	+ 5	V
I_{d1}, I_{d2}	Drain current			100	mA
P_{IN}	RF Input power			+ 10	dBm
T_{amb}	Ambient temperature		- 40	+ 85	$^{\circ}\text{C}$
T_j	Junction temperature			+ 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		- 55	+ 150	$^{\circ}\text{C}$

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-amb)}$	Thermal resistance from junction to ambient (DC power at T_{amb} max)	TBD	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS

$T_{amb} = + 25 \text{ }^{\circ}\text{C}$, $V_{d1}, V_{d2} = 3.3\text{V}$, $I_{d1} + I_{d2} = 20\text{mA}$

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
R_{Fin}	Input frequency		13		15	GHz
<i>Performances on wafer at $f_i = 14 \text{ GHz}$</i>						
V_{DD1}, V_{DD2}	Drain Supply voltage			+ 3.3		V
I_{D1}, I_{D2}	Drain Supply current	$V_{gg}=0\text{V}$		20		mA
G	Gain			25		dB
NF_{MIN}	Noise Figure			1.5		dB
P_{1dB}	1dB compression point			8		dBm
P_{sat}	Saturated power			9		dBm
$OIP3$	Output third order intercept point			TBD		dBm
$IMD3$	2 Carriers 3 dB below P_{1dB}			TBD		dBc
ISO_{rev}	Reverse Isolation	R_{FOUT}/R_{FIN}		-47		dB
S_{11}	Input reflection coefficient	50 Ohms		-11		dB
S_{22}	Output reflection coefficient	50 Ohms		-20		dB

(*) Measurement reference planes are the INPUT and OUTPUT plans of the CGY2125UH/C1 MMIC.



Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

CGY2125AUH/C1 have been measured on-wafer this method assure a full polarization conditions

S-PARAMETERS

Conditions: $V_{d1, d2} = 3.3V$, $I_{d1} + I_{d2} = 20mA$, $T_{amb} = + 25^{\circ}C$ (On Wafer measurements)

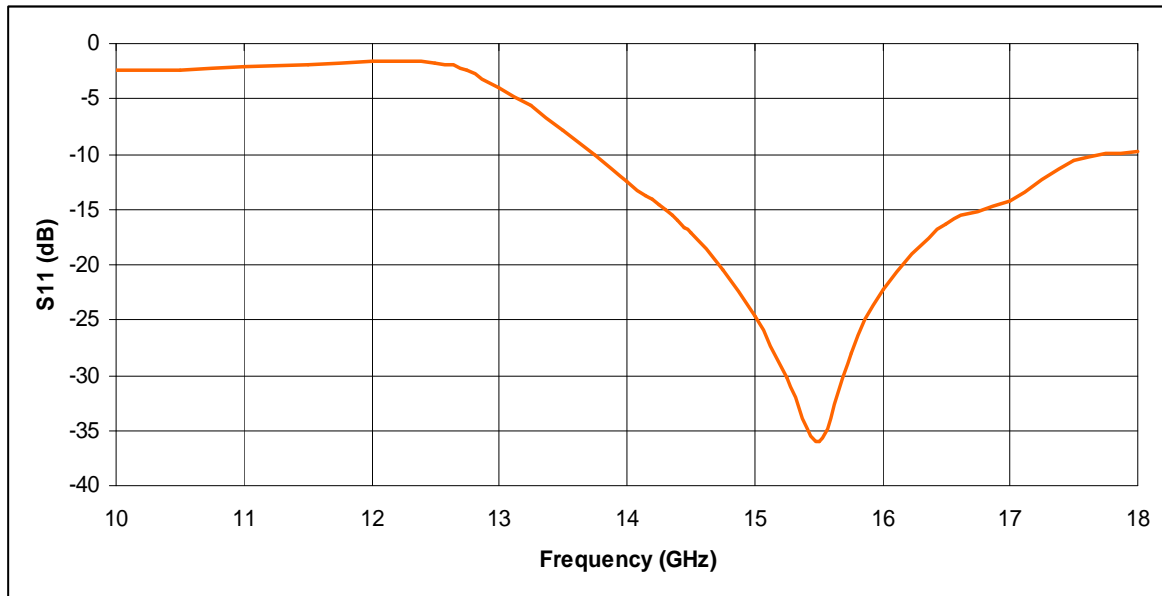


Figure 1 : S11 measurements

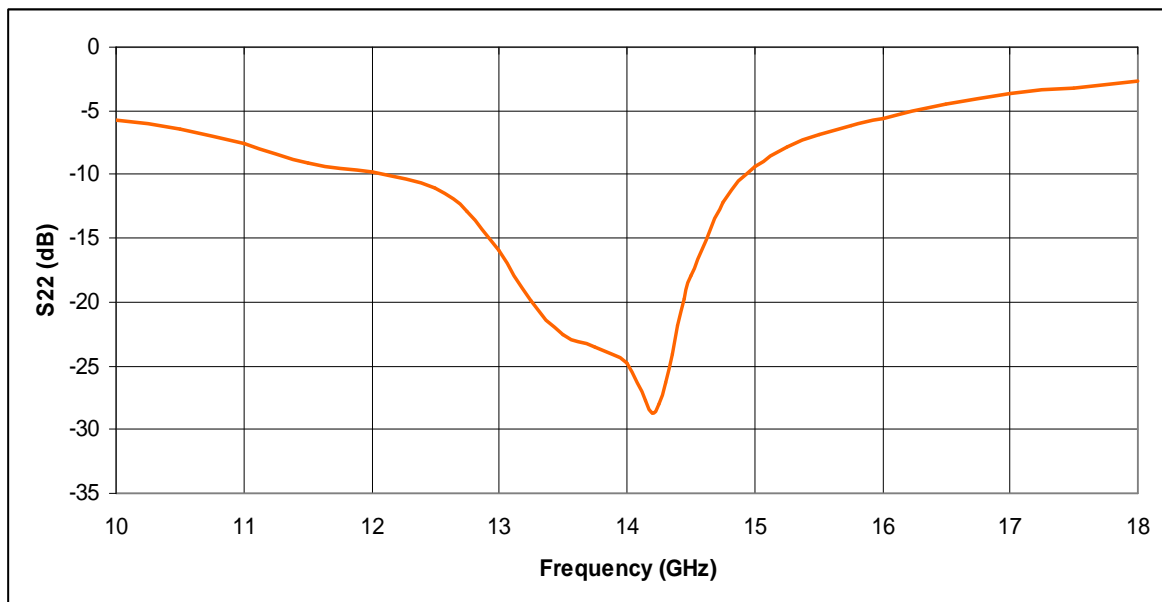
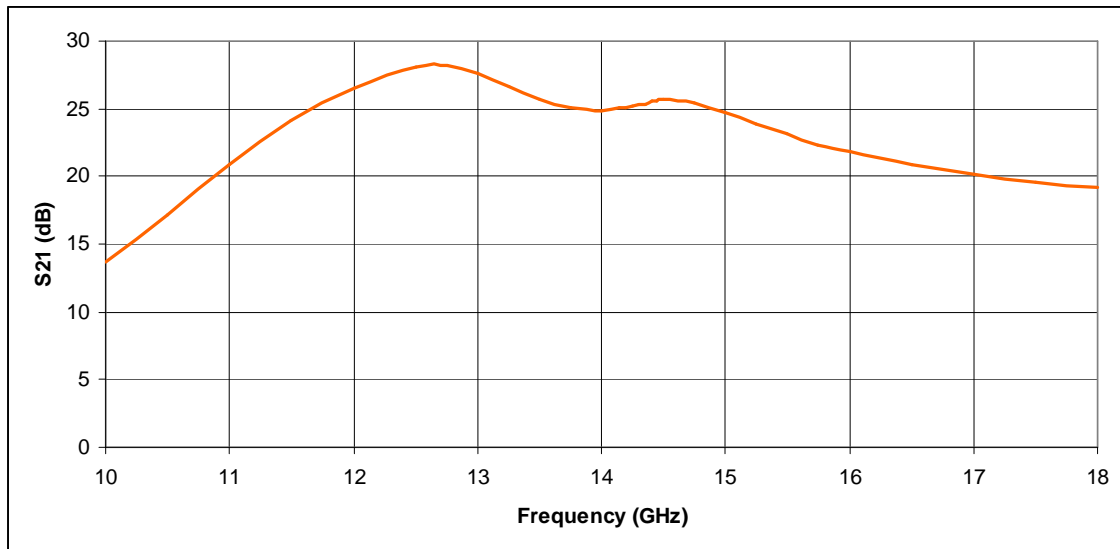
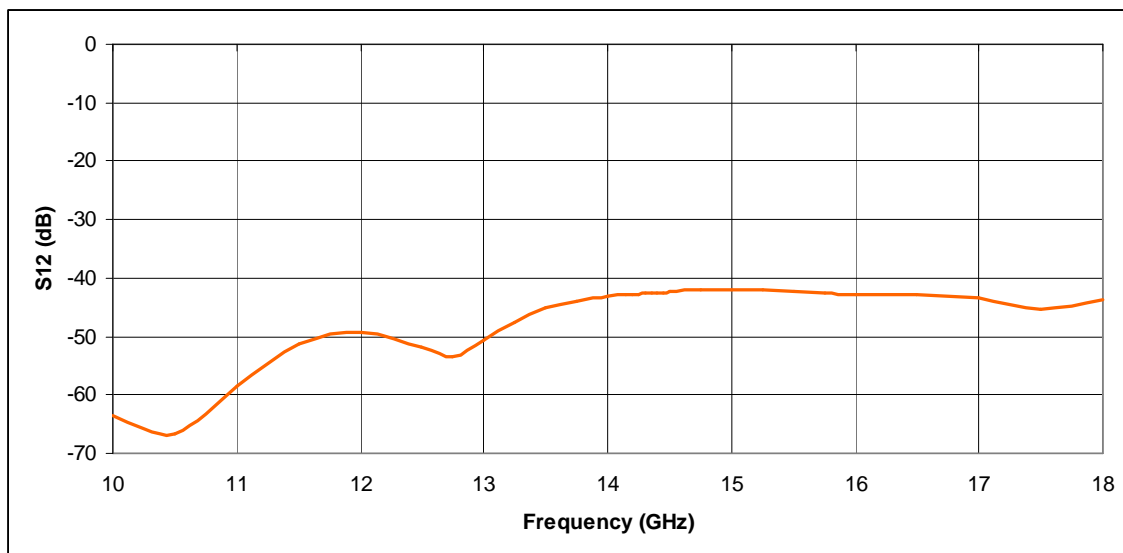


Figure 2 : S22 measurements


Figure 3 : Gain

Figure 4 : Reverse Isolation

S PARAMETERS

Conditions : $V_{d1}, V_{d2} = 3.3V$, $I_{d1} + I_{d2} = 20mA$, $T_{amb} = + 25^{\circ}C$ (On-Wafer measurements)

GHz	Mag S11	S11 Phase	Mag S21	S21 Phase	Mag S12	S12 Phase	Mag S22	S22 Phase
10.00	-2.39	143.7	13.63	-71.86	-63.47	172.6	-5.74	7.94
11.00	-2.12	76.9	20.86	-133.50	-58.44	2.78	-7.49	-10.52
12.00	-1.64	-18.25	26.49	144.21	-49.26	-107.8	-9.79	-20.05
13.00	-3.94	-122.4	27.56	48.61	-50.59	-114.6	-16.01	-51.64
14.00	-12.59	172.3	24.95	-9.70	-43.03	-160.2	-24.76	-27.88
15.00	-24.67	133.2	24.74	-74.73	-41.88	155.5	-9.38	109.51
16.00	-22.62	36.59	24.89	-125.81	-42.91	122	-5.55	64.91
17.00	-14.26	-82.57	20.12	-169.05	-43.46	92.22	-3.61	41.05
18.00	-9.73	-123.5	19.19	144.20	-43.77	92.96	-2.7	22.33

NOISE FIGURE

Conditions : $V_{d1}, V_{d2} = 3.3V$, $I_{d1} + I_{d2} = 20mA$, $T_{amb} = + 25^{\circ}C$ (On-Wafer measurements)

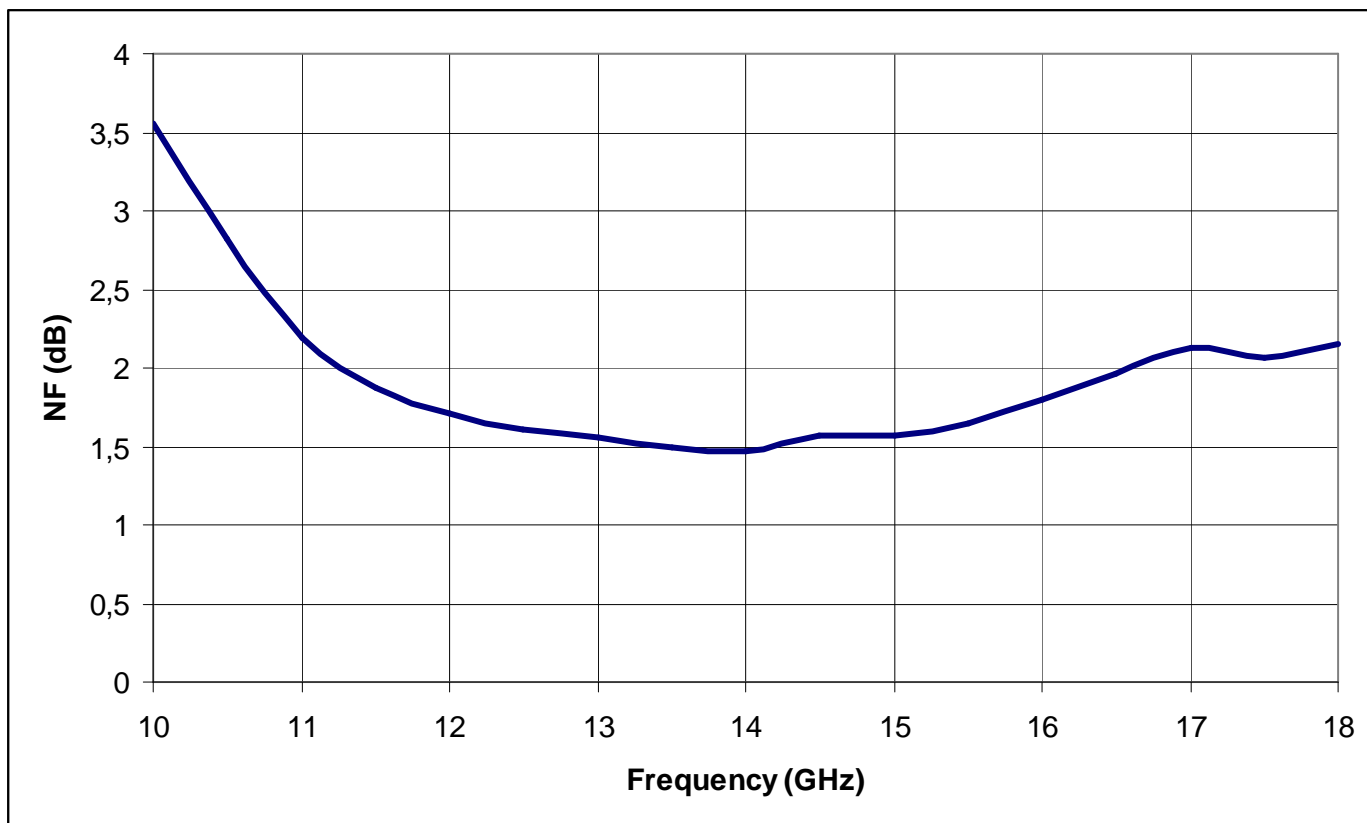


Figure 5 : Noise vs Frequency

APPLICATION SCHEMATIC

To prevent unstability of the customer design it is highly recommended to place small chip capacitors as near as possible to the CGY2125AUH/C1 die and to connect them with bondings as short as possible. An additional 10uF can also added on drain supplies in order to improve stability at low frequencies.

Additionally, a 10nF capacitor can be added on a drain connection. In the gate circuitry, a 500 Ω resistor may be added in serie to improve gate isolation and prevent unwanted oscillations. The resistors are introducing some low pass filtering in case of fast power switching using gate control architecture.

Depending on 50Ohms connected lines and associated tapers, many connections schemes can be studied/used regarding RFin and RFout connections.

RFin and RFout bondings can be doubled using two 25um wire bonding or one 50um ribbon.

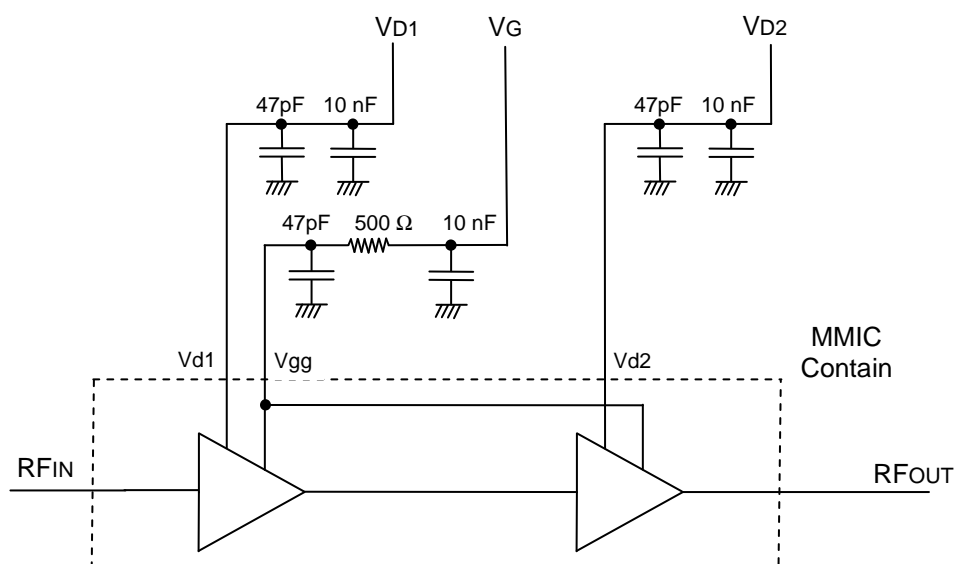


Figure 4 : CGY2125UH/C1 Application schematics

Component NAME	Value	Type	Comment
All 47pF capacitors	47pF	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die with bonding as short as possible
All 500 Ω resistors	500 Ω	Chip Resistor	Chip resistor US MICROWAVES RG1421-500-1% soldered close to the 47pF chip capacitor with bonding as short as possible
All 10nF capacitors	10nF	Chip Capacitor	MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520

Tableau 1 Components reference

DIE LAYOUT AND PIN CONFIGURATION

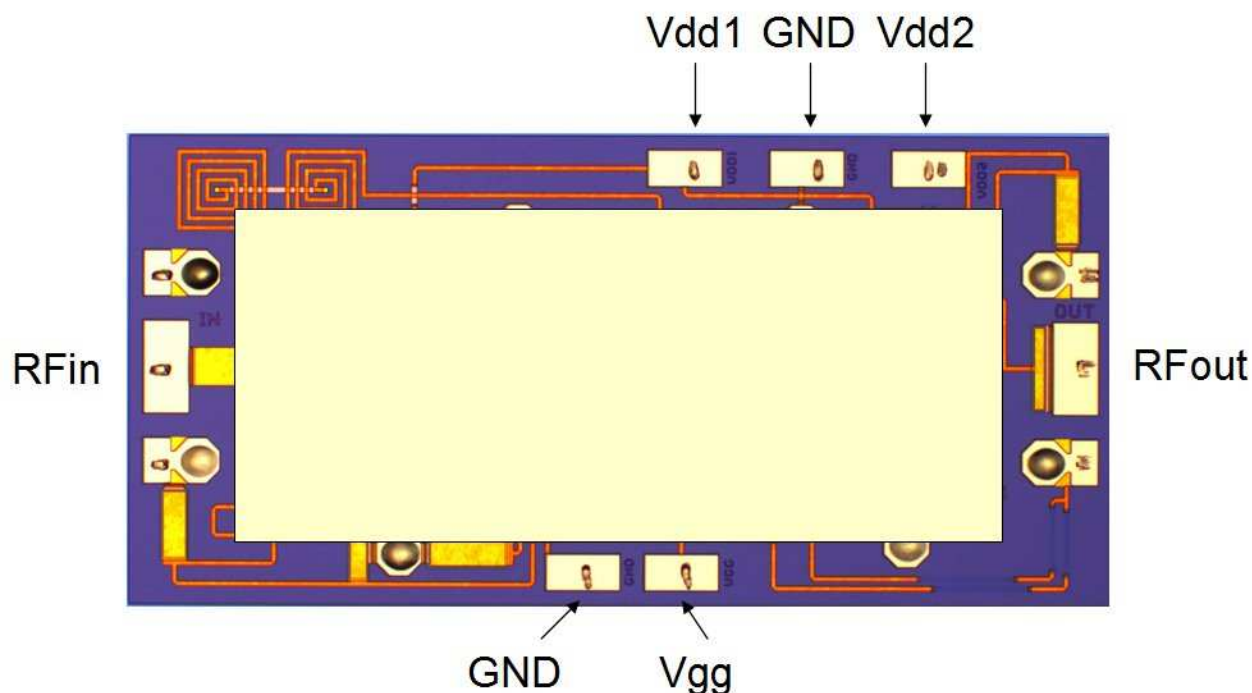


Figure 5 CGY2125UH/C1 Pad layout

PINOUT

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
Vd1	VD1	First stage Drain
Vd2	VD2	Second stage Drain
Vgg	VG1	First stage Gate
GND	BACKSIDE	Ground

Note :

In order to ensure good RF performances and stability It is key to connect to the ground the backside of the die.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on-wafer tested	11	-	2.2 x 1.1 x 0.1

ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2125A	UH	C1	-	On-Wafer measured Die

SOLDERING

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400°C.

DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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