

PRODUCT DATASHEET

CGY2178UH/C1

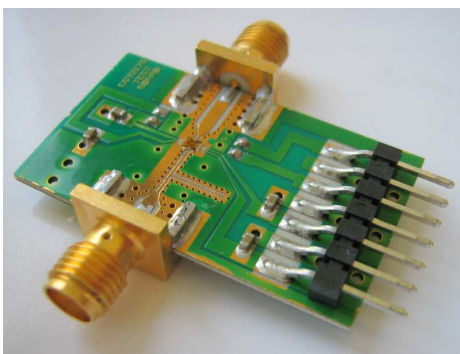
C band High Gain Low Noise Amplifier

DESCRIPTION

The CGY2178UH/C1 is a High Gain, Low Noise Figure MMIC amplifier designed for use with the OMMIC Integrated Core chip, Attenuator/Phase Shifter Chip Set or as a general purpose Low Noise Amplifier in band C.

The CGY2178UH/C1 uses a simple external matching circuit to provide excellent input matching and low noise figure between 5 and 6 GHz. All biasing, decoupling and output-matching networks are on chip.

The MMIC is manufactured with OMMIC's leading 0.18 μm PHEMT GaAs MMIC technology. The device is fully passivated.



CGY2178UH mounted on evaluation Board
(Rogers RO4003)

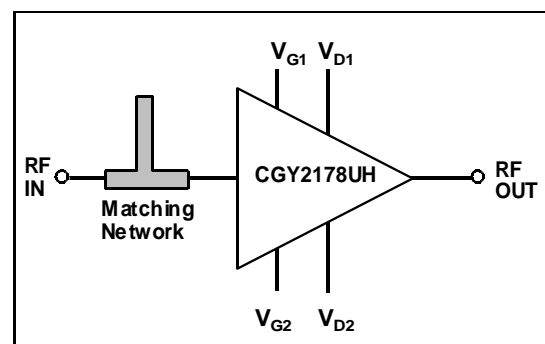
FEATURES

- ▶ C-band MMIC LNA
- ▶ 5 - 6 GHz operations
- ▶ S11, S22 < -15 dB (7.5% Bandwidth)
- ▶ S11, S22 : < - 10 dB (5–6 GHz)

NF (dB)	Gain (dB)	OIP3 (dBm)	OP1dB (dBm)	Bias conditions
1	30	22	15	3V 40 mA

(*) measured figures including noise contribution of connectors and biasing circuitry

- ▶ Circuit size : 1.5 mm x 1.6 mm, 100 μm thick
- ▶ Delivered as measured Known Good Die
- ▶ Uses a highly reliable PHEMT MMIC process
- ▶ Samples and Demonstration Boards Available
- ▶ Space and MIL-STD Available



Schematic diagram of the CGY2178UH

APPLICATIONS

- ▶ General performance LNA in the band 5–6 GHz
- ▶ C-band Active Antennas



LIMITING VALUES

$T_{amb} = + 23 \text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1}	Gate voltage of stage 1	V_{D1} open-circuited	-6	0	V
V_{D1}	Drain voltage of stage 1	V_{G1} open-circuited	0	+ 6	V
I_{D1}	Drain current of stage 1			40	mA
V_{G2}	Gate voltage of stage 2	V_{D2} open-circuited	-6	0	V
V_{D2}	Drain voltage of stage 2	V_{G2} open-circuited	0	+ 6	V
I_{D2}	Drain current of stage 2			60	mA
P_{IN}	Input power			5	dBm
T_{amb}	Ambient temperature		-40	+85	$^{\circ}\text{C}$
T_j	Junction temperature			+150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-55	+150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient ($T_a = 25 \text{ }^{\circ}\text{C}$)	235	$^{\circ}\text{C/W}$

CHARACTERISTICS

$V_{D1} = V_{D2} = 3 \text{ V}$, $I_{D1} = 10 \text{ mA}$, $I_{D2} = 30 \text{ mA}$, $T_{amb} = + 23 \text{ }^{\circ}\text{C}$, measured on reference board

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
f_i	Input frequency		5		6	GHz
<i>Supplies</i>						
V_{D1}	Supply voltage of stage 1			3		V
I_{D1}	Supply current of stage 1	$V_{G1} = - 0.5 \text{ V}$		10		mA
V_{D2}	Supply voltage of stage 2			3		V
I_{D2}	Supply current of stage 2	$V_{G2} = - 0.5 \text{ V}$		30		mA
<i>RF Performance at 5.3 GHz unless otherwise stated * of Reference Board</i>						
G	Gain			30		dB
NF	Noise Figure			1,05		dB
ISO_{rev}	Reverse Isolation	OUT/IN		40		dB
OIP3	Output third order intercept point			22		dBm
P_{1dB}	Output Power @ 1dB gain compression			15		dBm
S_{11}	Input reflection coefficient	50 Ω source		-15		dB
S_{22}	Output reflection coefficient	50 Ω load		-15		dB

(*) Measurement reference planes are the INPUT and OUTPUT SMA connectors.



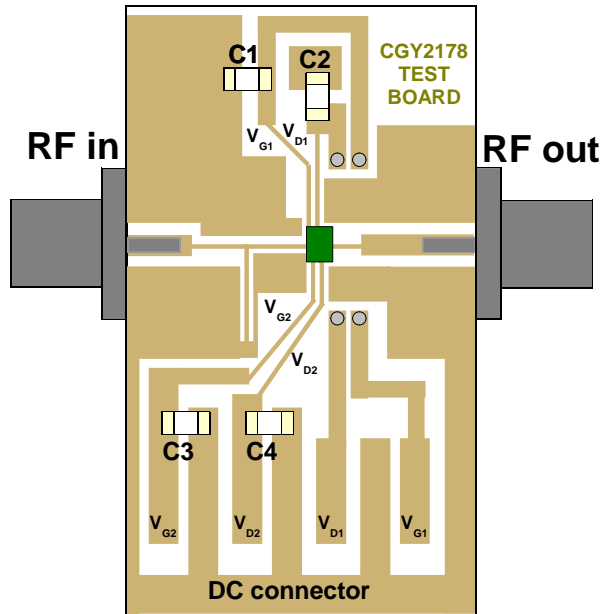
Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

S-PARAMETERS
 $V_{D1} = V_{D2} = 3 \text{ V}$, $I_{D1} = 10 \text{ mA}$, $I_{D2} = 30 \text{ mA}$, $T_{\text{amb}} = + 23 \text{ }^{\circ}\text{C}$, on wafer (bare die) measurement

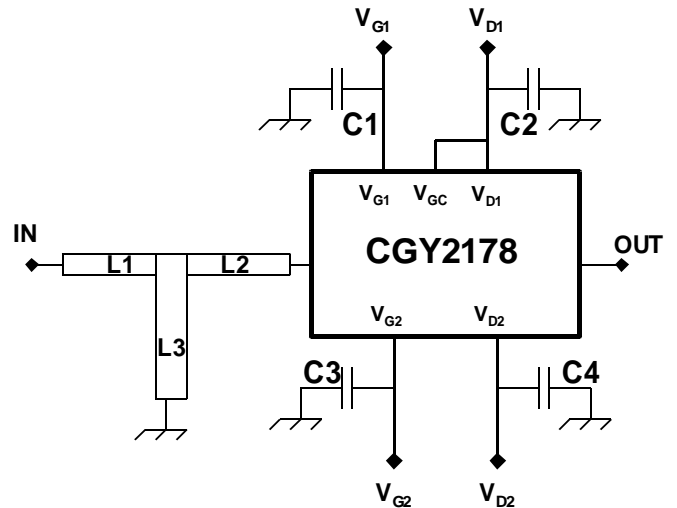
Frequency (GHz)	S11	Ang S11 (°)	S21	Ang S21 (°)	S12	Ang S12 (°)	S2 2	Ang S22 (°)
0,5	0,98816	-4,08200	0,93092	3,76200	0,00056	-144,03300	0,81973	0,00000
1	0,97955	-8,28400	0,34051	52,94300	0,00082	68,27700	0,88330	0,00000
1,5	0,95878	-11,92600	1,11874	115,32000	0,00020	29,82400	0,82409	0,00000
2	0,93946	-15,47500	3,59868	90,15300	0,00055	11,39600	0,57208	0,00000
2,5	0,91973	-18,54500	4,23393	69,75300	0,00023	-125,81400	0,52646	0,00000
3	0,89965	-21,45200	6,19907	56,52200	0,00062	-40,84100	0,49284	0,00000
3,5	0,87913	-24,21800	9,03832	38,92600	0,00069	-137,47900	0,42538	0,00000
4	0,85611	-27,43800	12,58419	19,70700	0,00077	-114,81100	0,37014	0,00000
4,5	0,82577	-30,72900	17,54876	-5,63200	0,00180	-160,23700	0,30325	0,00000
5	0,78047	-33,07700	22,52908	-40,34500	0,00208	-178,66300	0,26332	0,00000
5,1	0,76341	-34,26800	22,84354	-48,06600	0,00225	173,11500	0,26282	0,00000
5,2	0,76915	-35,21000	23,14307	-55,75800	0,00233	164,23700	0,26602	0,00000
5,3	0,76920	-34,53900	23,31013	-63,76800	0,00247	154,03400	0,27062	0,00000
5,4	0,75278	-33,74100	22,67221	-70,96400	0,00256	153,30800	0,27398	0,00000
5,5	0,73431	-32,63500	22,21604	-78,75000	0,00293	146,81300	0,28154	0,00000
5,6	0,72276	-33,55600	21,52937	-85,64200	0,00303	148,85200	0,28416	0,00000
5,7	0,72620	-34,10900	20,71187	-92,17800	0,00289	146,58200	0,28861	0,00000
5,8	0,73453	-33,37100	19,87145	-98,01400	0,00244	141,57400	0,29118	0,00000
5,9	0,73731	-32,22700	19,09359	-103,54800	0,00217	130,57600	0,29282	0,00000
6	0,72564	-31,57600	18,13381	-108,37300	0,00221	121,98600	0,29258	0,00000
6,5	0,73215	-32,19600	14,38786	-129,11700	0,00277	113,71300	0,27902	0,00000
7	0,73782	-33,35300	11,65372	-146,96000	0,00202	95,42900	0,26964	0,00000
7,5	0,73457	-34,67800	9,47557	-159,93900	0,00246	96,56600	0,24687	0,00000
8	0,73331	-35,82200	7,78423	-169,91400	0,00215	74,31100	0,22127	0,00000
8,5	0,73712	-37,96300	6,80575	-178,69700	0,00259	89,75100	0,20023	0,00000
9	0,73165	-39,56400	5,94930	172,71400	0,00216	67,21400	0,17798	0,00000
9,5	0,72918	-41,10100	5,15002	164,08500	0,00240	75,19900	0,16324	0,00000
10	0,73117	-42,30900	4,69940	158,45200	0,00184	67,41300	0,15014	0,00000

REFERENCE BOARD

Assembly drawing



Circuit Diagram



Bill of materials

INPUT matching (see note 1):

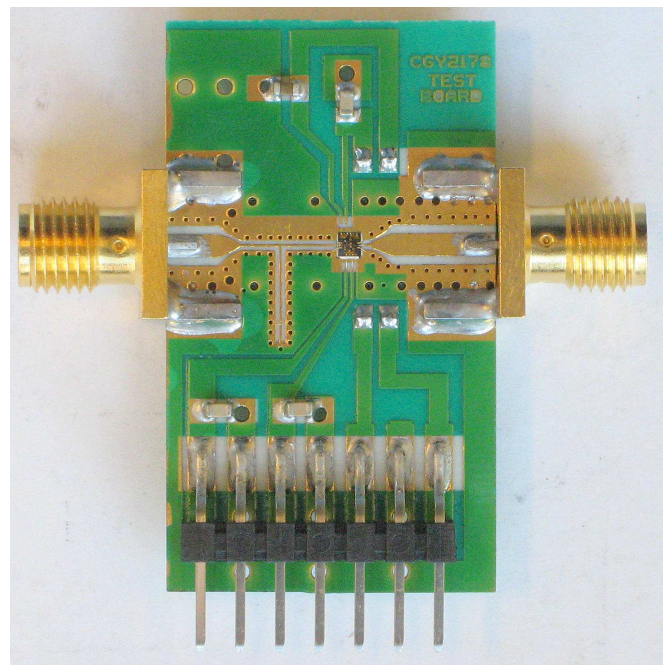
Optimised for 5300 MHz. L1, L2 and L3 are coplanar transmission lines.

Component	Length (µm)	Width (µm)	Gap (µm)
L1	2600	200	200
L2	3500	200	200
L3	4000	200	200

Note 1: Dimensions are given for Rogers RO4003 substrate material. (Height = 800 µm, E_r = 3.4).

Component	Value	Reference
C1, C2, C3, C4	100 nF	0603

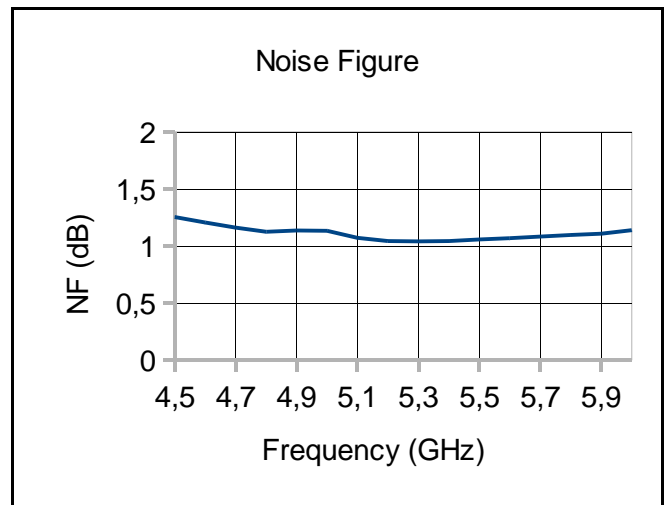
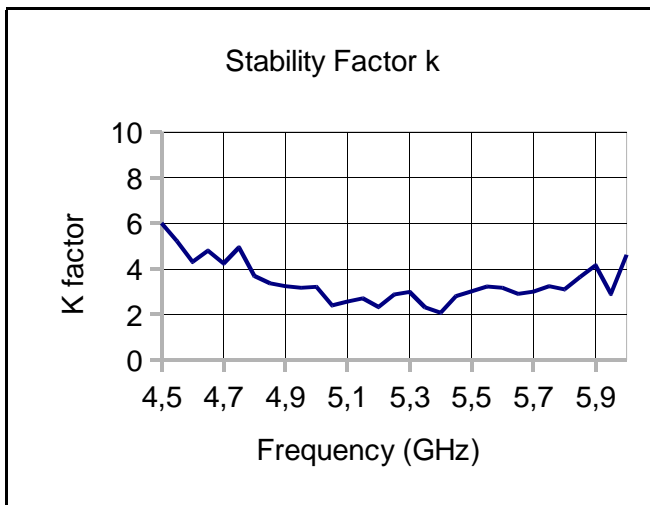
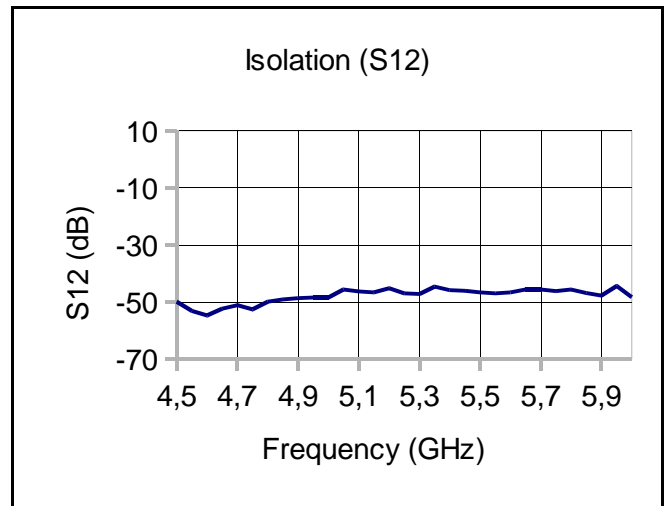
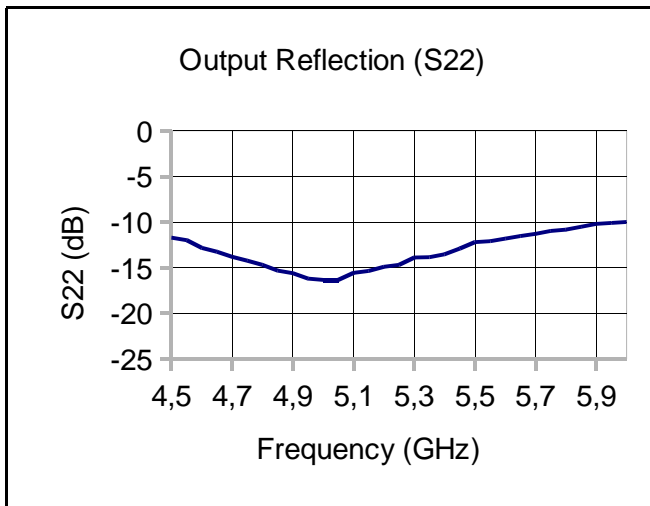
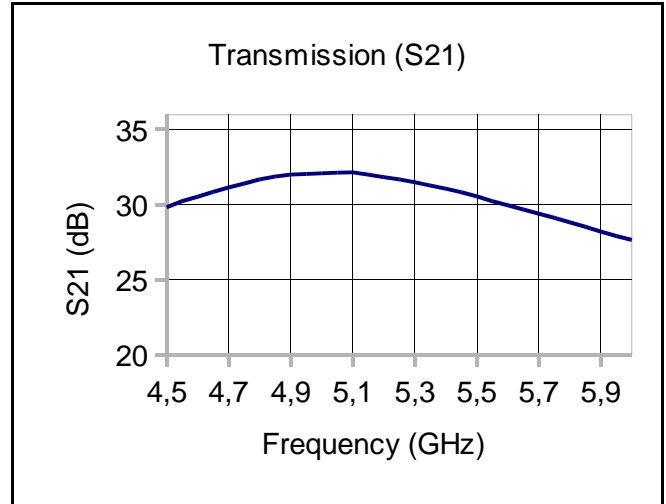
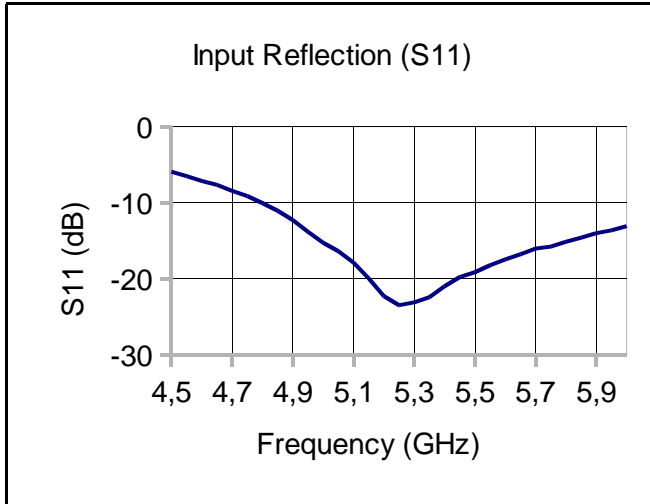
CGY2178UH Reference Board



MEASURED PERFORMANCE OF EVALUATION BOARD OPTIMISED FOR 5.3 GHZ

 Conditions : $V_{D1} = V_{D2} = 3 \text{ V}$, $I_{D1} = 10 \text{ mA}$, $I_{D2} = 30 \text{ mA}$, $T_{\text{amb}} = + 23 \text{ }^\circ\text{C}$.

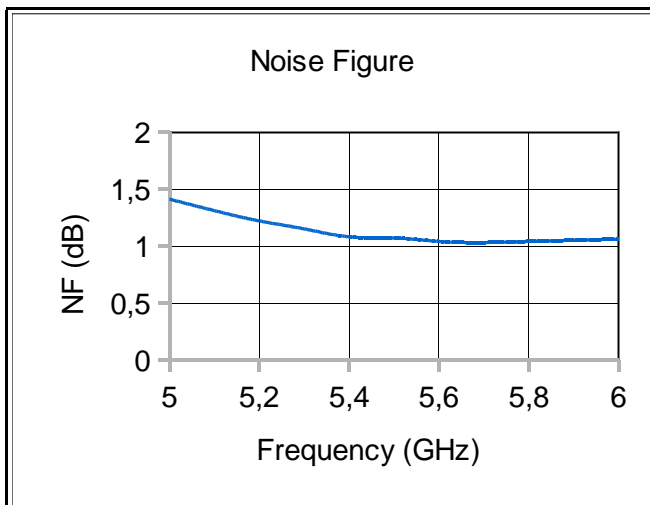
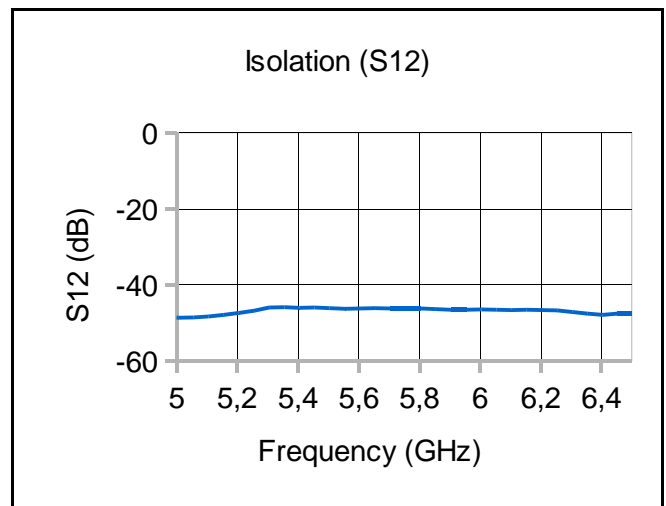
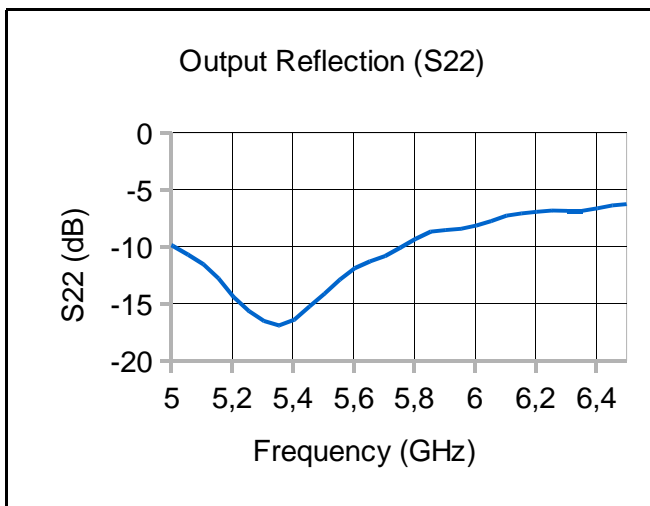
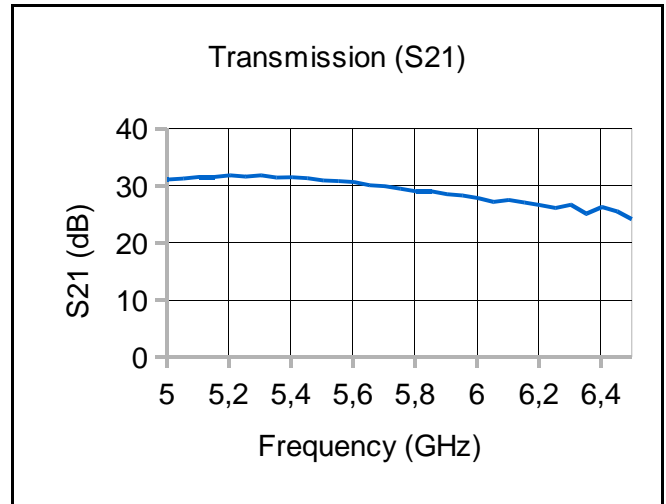
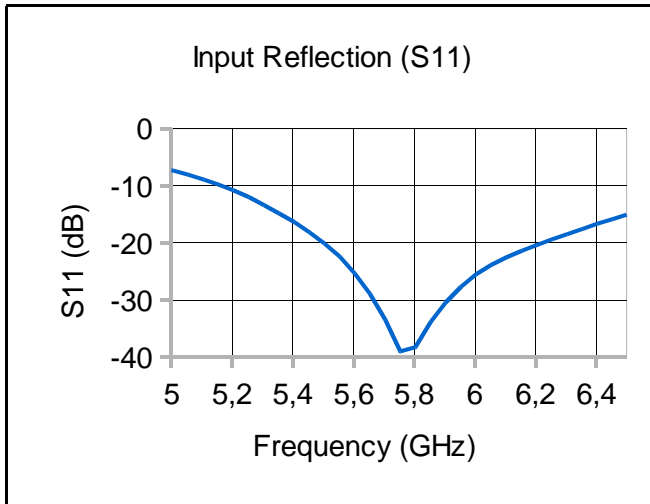
Measurements include RF connector contributions.



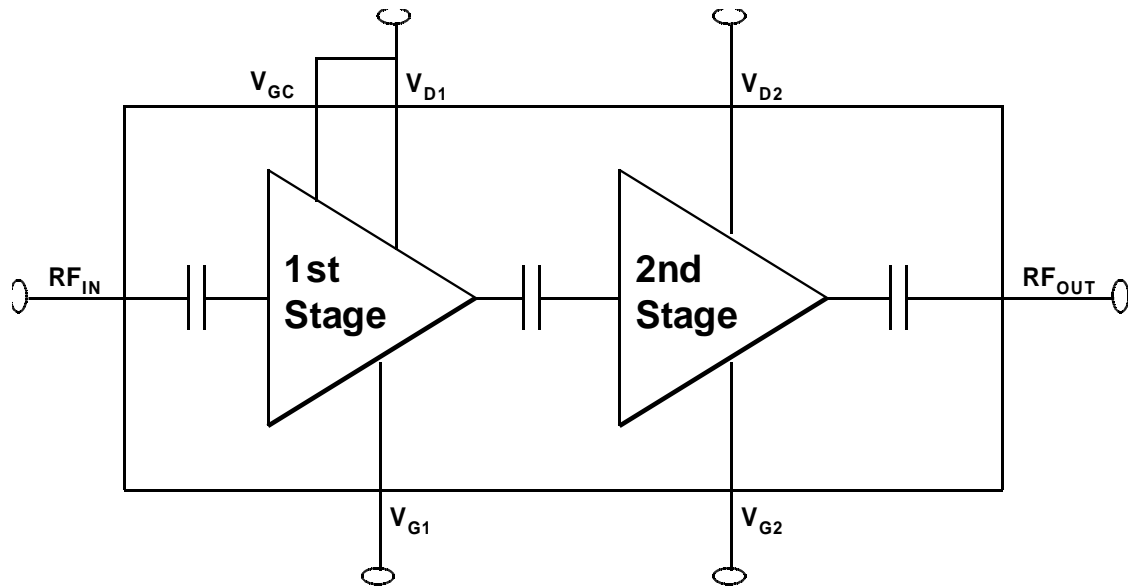
MEASURED PERFORMANCE OF EVALUATION BOARD OPTIMISED FOR 5.8 GHZ

 Conditions : $V_{D1} = V_{D2} = 3 \text{ V}$, $I_{D1} = 10 \text{ mA}$, $I_{D2} = 30 \text{ mA}$, $T_{\text{amb}} = + 23 \text{ }^\circ\text{C}$.

Measurements include RF connector contributions.



BLOCK DIAGRAM



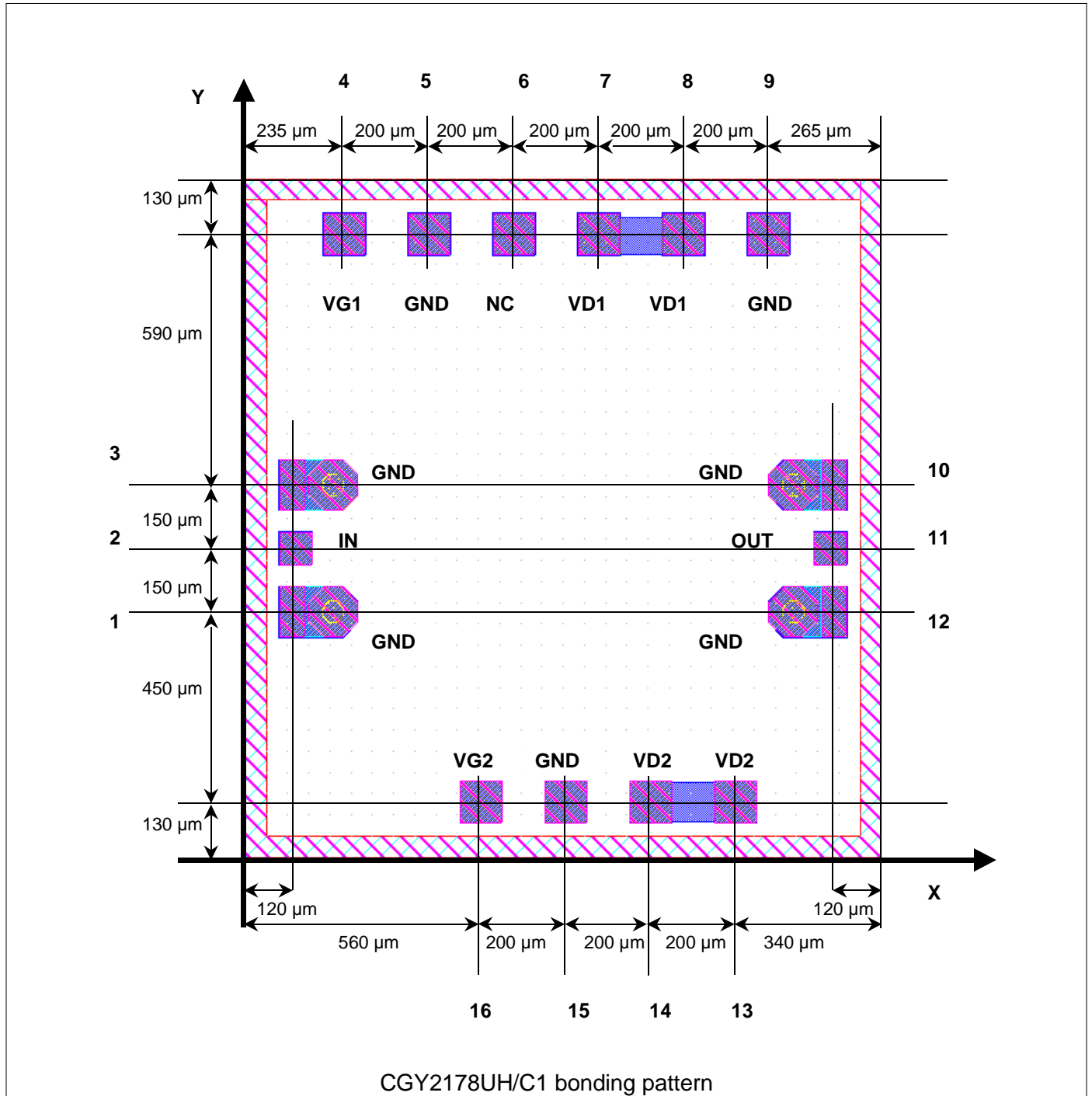
PINNING

Symbol	Pin	Description
GND	1, 3, 5, 9, 10, 12, 15	Ground All pins are connected to chip back-side by on-chip via-holes
IN	2	RF INPUT
OUT	11	RF OUTPUT
V _{G1}	4	Stage 1 : Gate Biasing
V _{D1}	7, 8	Stage 1 : Drain Biasing
V _{G2}	16	Stage 2 : Gate Biasing
V _{D2}	13, 14	Stage 2 : Drain Biasing
V _{GC}	6	Connected to V _{D1}

MECHANICAL INFORMATION

PARAMETER		VALUE
Size		1500 x 1600 μm (Tolerance : +/- 15 μm)
Thickness		100 μm
Backside material		TiAu
Passivation		PECVD deposited Si ₃ N ₄
Bonding pad dimensions	GND, VG1, VGC, VD1, VG2, VD2	100 x 100 μm
	IN, OUT	80 x 80 μm

BONDING PADS



DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

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ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2178	UH	C1		MMIC C band LNA
CGY2178	UH	C1	REFBOARD	Single Ended Reference Board



Document History : Version 1.2, Last Update 21/4/2010