Preliminary DATASHEET

Rev 0.3

CGY2145UH/C1

Low Noise 0.5-45GHz Wide Band Amplifier

DESCRIPTION

The CGY2145UH is a GaAs very wide band Low Noise Amplifier MMIC.

The CGY2145UH has a low noise figure of 2,6dB at 20GHz and a P1dB of 18dBm at 20Ghz. This LNA exhibits a small signal gain of 12.7dB from 100MHz to 28GHz and >12dB up to 44GHz.

The CGY2145UH features single-ended input and output and operates with a +5.0V supply voltage via an external bias tee.

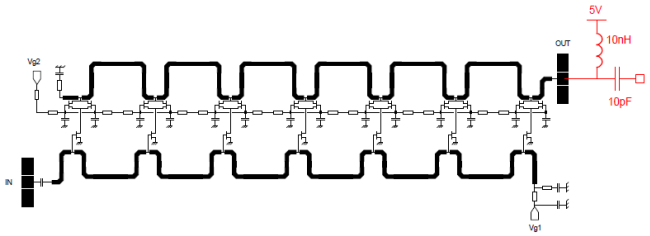
The MMIC is manufactured using OMMIC's qualified 0.13 µm PHEMT GaAs D01PH technology. The D01PH process has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

APPLICATIONS

- Radar
- Space application
- Telecommunication
- Instrumentation
- General purpose Low Noise Amplifier

FEATURES

- Wide frequency range : 0.5 – 45 GHz
- 12.7 dB small signal gain
- Power consumption: 420mW
- Input Return Loss : > 13.5dB at 20GHz
- Output Return Loss : > 16.5dB at 20GHz
- P_{1dB} = 18 dBm at 20GHz
- NF=2,6dB at 20GHz
- Nf_{min}=1,8dB at 9GHz
- Chip size = 1850 x 1060 µm
- Tested, Inspected Known Good Die (KGD)



- Space and MIL-STD Available

Block Diagram of the CGY2145UH
Wide Band Low Noise Amplifier

RoHS Compliant

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LIMITING VALUES

Tamb = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DD}	Supply voltage		-0.5	+8	V
I_{DD}	Supply current			240	mA
V_{g1}	Gate supply voltage1		-5	0	V
V_{g2}	Gate supply voltage2		-5	5	V
T_{stg}	Storage temperature		-55	+150	° C
T_j	Junction temperature			+150	° C
T_{amb}	Ambient temperature		-10	+85	° C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient (T_a = 25 °C)	TBD	° C/W

DC CHARACTERISTICS

T_{amb} = 25 °C, V_{DD} = 5 V, R_L = 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		+4.75	+5.0	+5.25	V
I_{DD}	Supply current			85	90	mA
V_{g1}	Gate supply voltage1	See note 1	-3	-0.3	0	V
V_{g2}	Gate supply voltage2		0.0	3.0	3.0	V

NOTE

1-V_{g1} determines the typical drain current. V_{g1} should be raised from –3V until the drain DC current reaches 85 mA.

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AC CHARACTERISTICS

T_{amb} = 25 °C, V_{DD} = 5 V, V_{g2} = 2,3 V, I_{DD} = 85 mA, V_{g1} = -0,3 V, R_L = 50 Ω; The specifications mentioned below are measured on-wafer, using 50 Ω RF probes. Unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Gain	Reference Gain	F = 3 GHz (see note 1)		12.6		dB
Gain ripple	See note 2	F = 100 MHz to 35 GHz	-0.6		+1.5	dB
		F = 35 GHz to F_C	-1			dB
F_C	High frequency cut-off	$Gain_{3GHz}$ – 3dB	44	46		GHz
F_{C_low}	Low frequency cut-off	See note 3			50	KHz
S11	Input return loss	F = 100 MHz to 22 GHz		-16	-13.5	dB
		F = 22 GHz to 35 GHz		-14	-12	dB
		F = 35 GHz to 45 GHz		-11.5	-10	dB
S22	Output return loss	F = 100 MHz to 30 GHz	-35	-16	-15	dB
		F = 30 GHz to 40GHz		-13	-10	dB
		F = 40 GHz to 45 GHz		-14	-12	dB
NF	Noise Figure	F = 5 GHz to 35 GHz		<4.5		dB
P1dB	Output P1dB	F = 1 GHz to 30 GHz		18		dBm
K	Microwave stability factor. T_{amb} = -10°C to +85°C	All passive source and loads	1.2			

NOTE

1-Measurement is guaranteed by correlation down to the lower frequency cut-off. 3 GHz is specified as a reference for convenience of measurement.

2-Low frequency gain ripple assumes the use of drain decoupling close to the chip, as proposed on the figure 1 and 2.

3-The input and output are DC coupled. The low frequency cut-off is set by the choice of the input blocking capacitor or by the output bias tee used for drain current supply voltage.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/001/PG” contains more information on the precautions to take.

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MEASURED PERFORMANCE

S-PARAMETERS

T_{amb} = 25 °C, V_{DD} = 5 V, V_{g2} = 2.3 V, I_{DD} = 85 mA, V_{g1} = -0.3 V, on wafer measurements

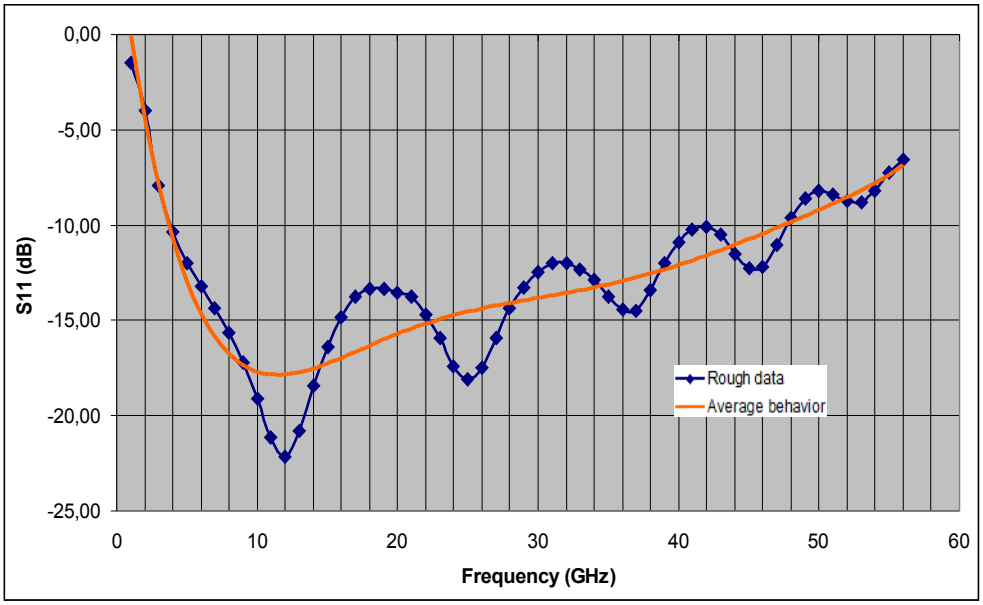

Figure 1 : S11 vs Frequency

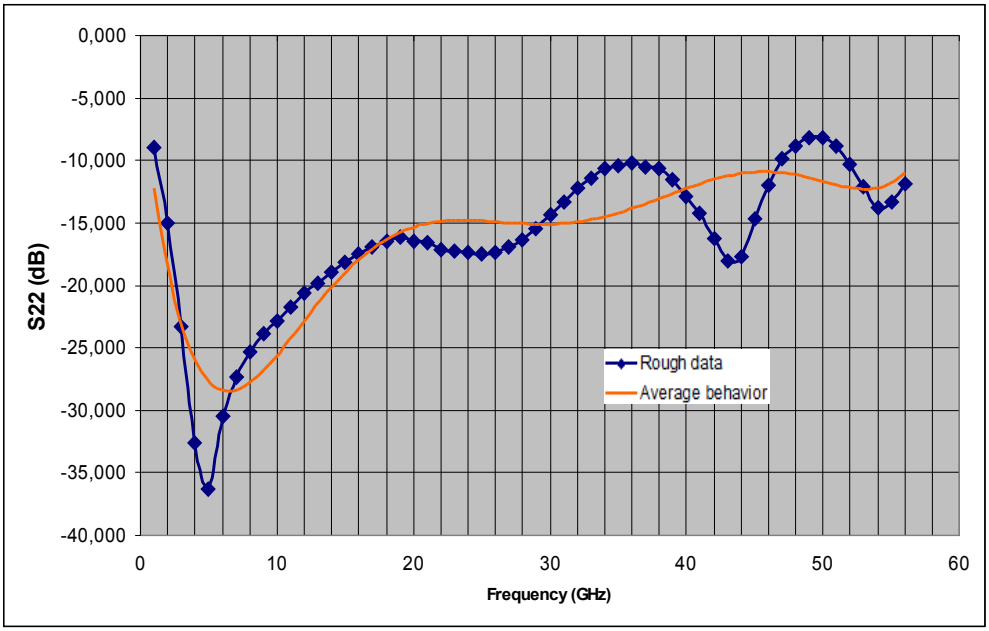

Figure 2 : S22 vs Frequency

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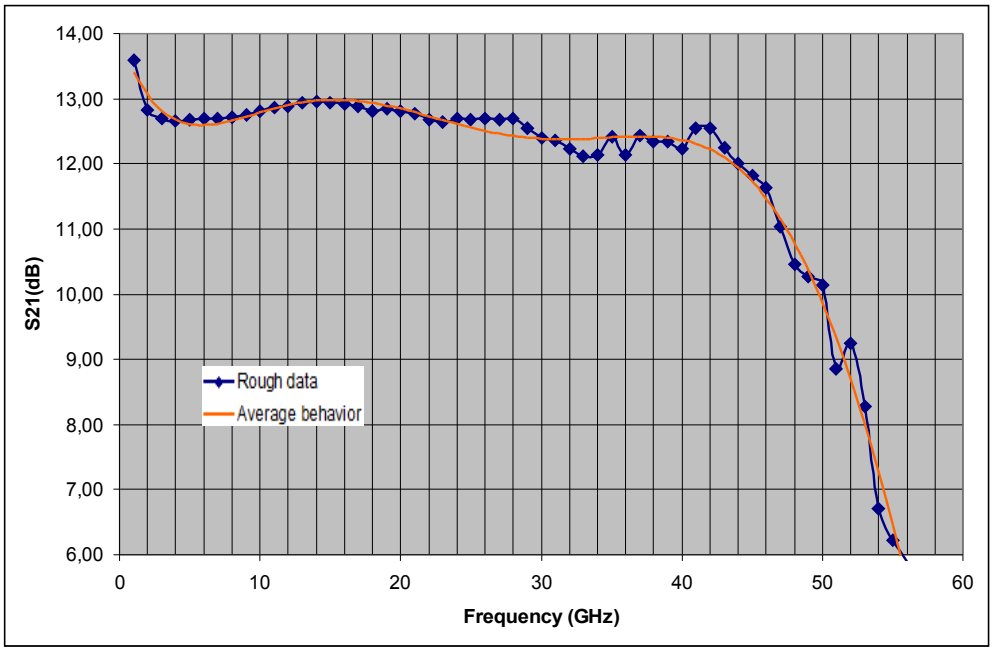

Figure 3 : S21 vs Frequency

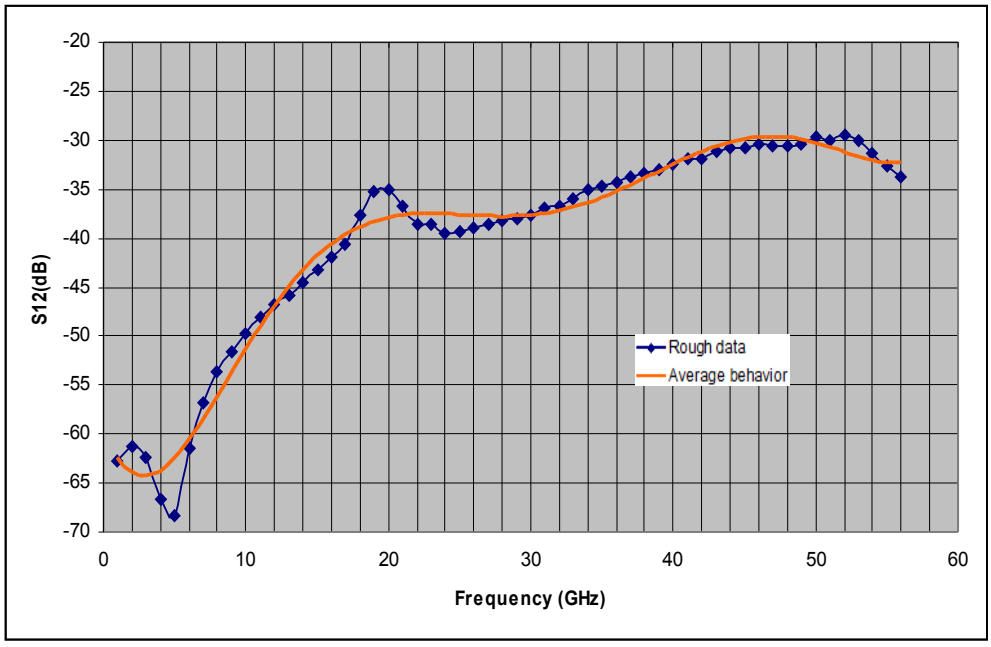

Figure 4 : S12 vs Frequency

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CGY2145UH TYPICAL SCATTERING PARAMETERS

T_{amb} = 25 °C, V_{DD} = 5 V, V_{g2} = 2.3 V, I_{DD} = 85 mA, V_{g1} = -0.3 V, on wafer measurements

Frequency (GHz)	Mag(S11)	Phase(S11)	Mag(S21)	Phase(S21)	Mag(S12)	Phase(S12)	Mag(S22)	Phase(S22)
0.5	0.83	-39.129	4.9	161.933	0.001	39.617	0.36	-71.513
1	0.62	-64.882	4.5	159.772	0.001	13.964	0.17	-90.545
3	0.30	-111.362	4.42	134.838	0.001	10.157	0.012	-111.974
5	0.22	-136.476	4.4	106.799	0.001	60.449	0.04	27.806
7	0.17	-154.700	4.4	78.501	0.002	53.731	0.06	11.611
9	0.11	-163.162	4.43	49.854	0.003	34.521	0.08	-1.840
11	0.75	-138.477	4.49	20.399	0.004	12.218	0.1	-10.827
13	0.11	-108.098	4.5	-9.698	0.006	-7.300	0.12	-20.421
15	0.18	-115.152	4.47	-39.892	0.008	-27.707	0.14	-30.835
17	0.22	-131.971	4.4	-70.134	0.014	-53.462	0.15	-43.181
19	0.21	-142.712	4.38	-100.474	0.017	-120.628	0.15	-54.052
21	0.19	-155.426	4.3	-130.883	0.012	-159.462	0.14	-59.597
23	0.13	-150.933	4.31	-161.029	0.01	177.173	0.15	-59.858
25	0.14	-125.916	4.29	167.343	0.01	154.398	0.15	-56.311
27	0.2	-121.564	4.28	134.921	0.01	133.304	0.16	-52.967
29	0.25	-131.618	4.10	102.896	0.012	113.187	0.2	-52.483
31	0.26	-145.222	4.04	70.524	0.014	87.153	0.26	-60.541
33	0.23	-152.956	3.97	38.750	0.017	57.227	0.3	-73.157
35	0.2	-148.386	3.98	4.322	0.02	23.778	0.32	-88.980
37	0.22	-135.714	4.05	-30.164	0.021	-12.166	0.28	-103.086
39	0.3	-143.463	3.94	-66.852	0.024	-45.372	0.21	-114.954
41	0.32	-157.881	4.03	-105.112	0.025	-82.823	0.13	-107.436
43	0.25	-167.751	3.82	-144.218	0.027	-129.446	0.16	-63.470
45	0.26	-156.783	3.61	174.542	0.028	-164.271	0.29	-64.051
47	0.34	-161.158	3.11	134.561	0.027	155.463	0.38	-83.666
49	0.38	-177.460	2.9	89.630	0.03	110.967	0.38	-105.400
51	0.36	173.818	2.53	52.261	0.03	69.605	0.29	-115.423
53	0.41	169.027	1.93	7.411	0.022	21.043	0.24	-104.675
55	0.48	156.393	1.8	-28.774	0.017	-19.316	0.3	-93.366
57	0.53	137.785	1.53	-68.926	0.014	-39.167	0.4	-99.374
59	0.59	118.530	1.57	-121.766	0.013	-75.473	0.43	-114.821
61	0.6	98.601	1.42	-172.141	0.014	-117.390	0.38	-118.706
63	0.57	80.471	1.19	125.633	0.014	-166.714	0.45	-113.246
65	0.59	65.262	0.84	62.095	0.014	134.441	0.59	-125.374

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NOISE PARAMETERS

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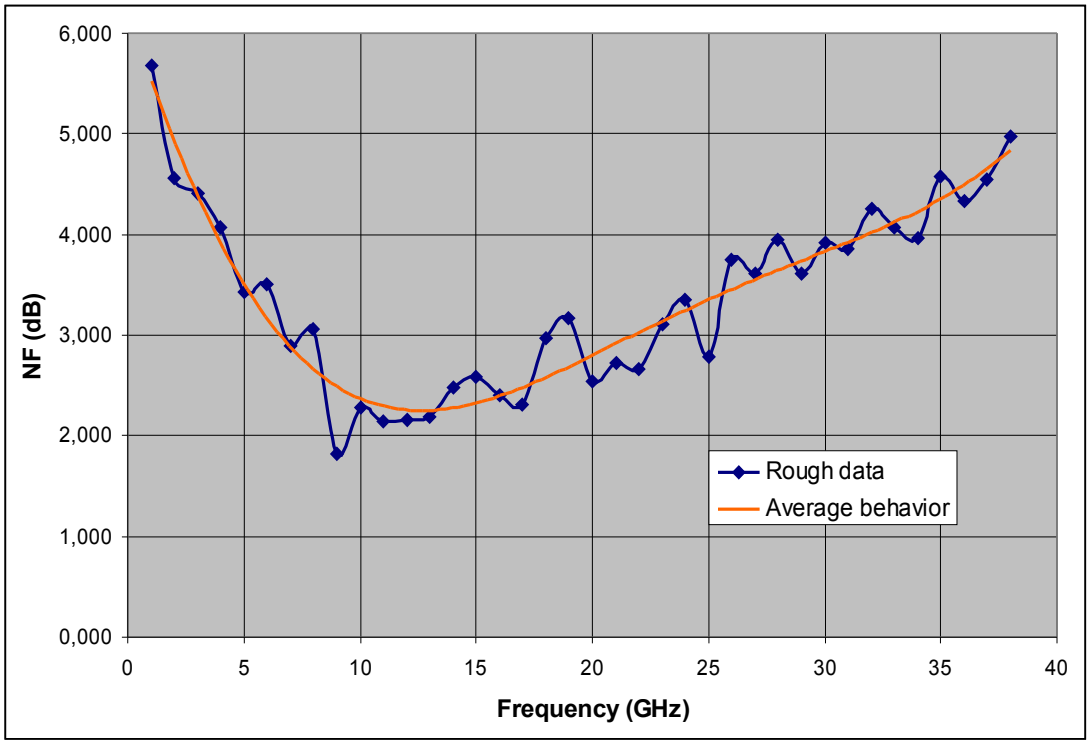

Figure 4 : NF vs Frequency measurments

APPLICATION INFORMATION

OPERATING AND HANDLING INSTRUCTIONS

The CGY2145UH is a very high performance GaAs device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

The following power supply sequence is recommended.

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting V_{g1} to –4.5 V and V_{g2} to 0.0 V.
c) Increase V_{dd} = 5.0 V while monitoring the drain current.
d) Increase V_{g2} to 2.3 V
e) Increase V_{g1} slowly from – 3V until the drain current reaches 84 mA.
f) Apply the RF input signal.

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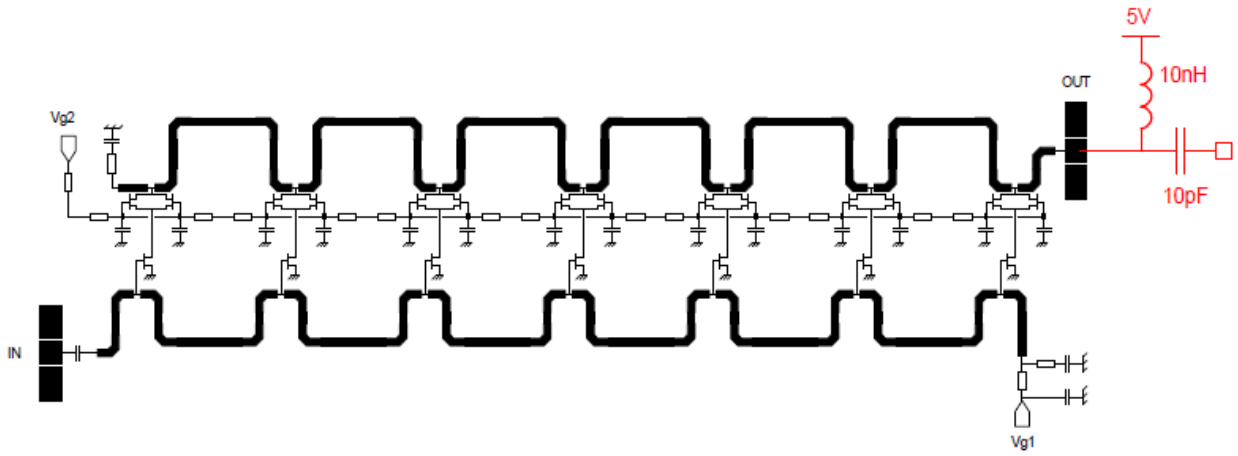
BLOCK DIAGRAM AND PAD CONFIGURATION



CGY2145UH Block Diagram

PAD POSITION

SYMBOL	PAD	COORDINATES (1)		DESCRIPTION
		Y	X	
GND	1	160	130	Connected to ground with on-chip via hole
IN	2	310	130	RF input
GND	3	460	130	Connected to ground with on-chip via hole
V_{g2}	4	930	130	Gate supply voltage 2, must be decoupled to ground using external capacitor(s)
GND	5	930	430	Connected to ground with on-chip via holes
GND	6	900	1720	Connected to ground with on-chip via hole
OUT	7	750	1720	RF output , used to connect V_{DD} via bias Tee
GND	8	600	1720	Connected to ground with on-chip via hole
V_{g1}	9	130	1380	Gate supply voltage 1, must be decoupled to ground using external capacitor(s)
GND	10	130	1080	Connected to ground with on-chip via hole

NOTE

1-All x and y coordinates in µm represent the position of the centre of the pad with respect to the lower left corner of the chip layout (see the bonding pattern).

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MECHANICAL INFORMATION

PARAMETER		VALUE
Size		1850 x 1060 µm (Tolerance : +/- 15 µm)
Thickness		100 µm
Backside material		TiAu
Passivation		PECVD deposited Si_3N_4
Bonding pad dimensions	GND, V_{g1}, V_{g2}, IN, OUT	100 x 100 µm

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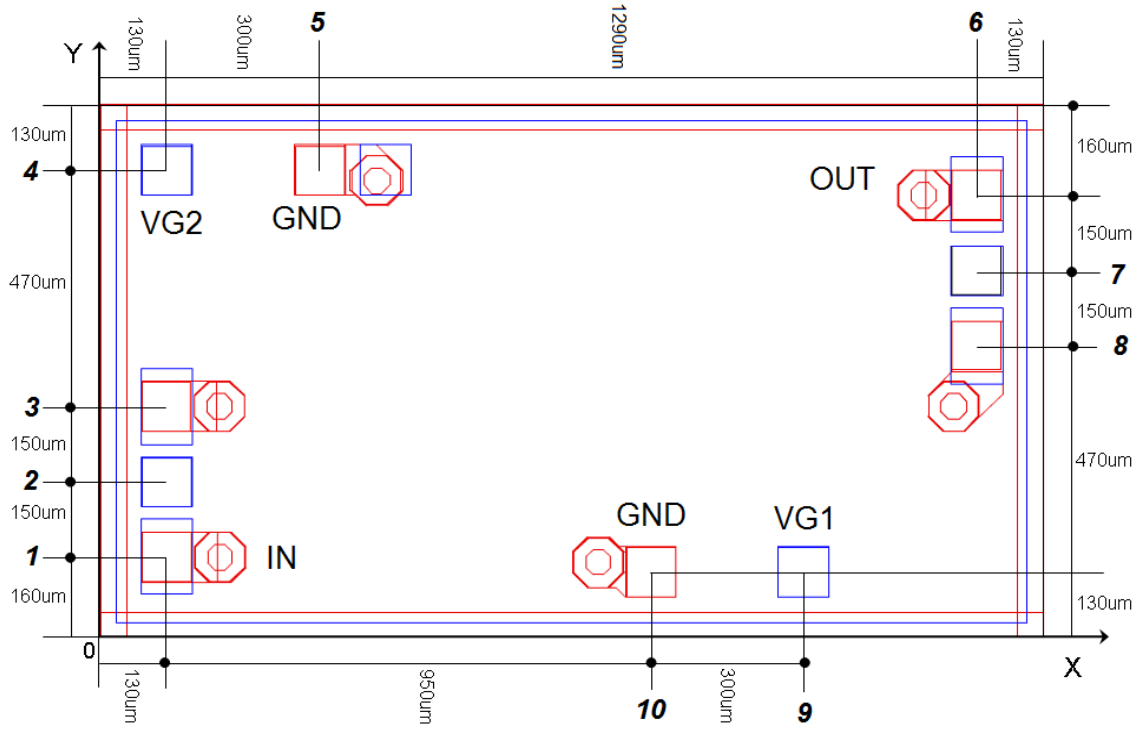
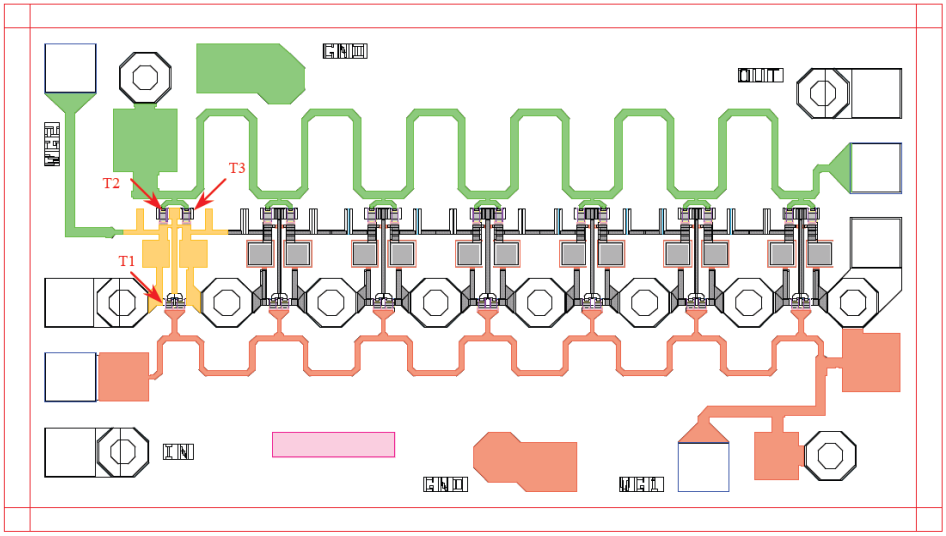
BONDING PADS



CGY2145UH bonding pattern



Design of CGY2145UH

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DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

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